

Specialty Foundry Technology and Design Enablement for RF, High Performance Analog, and Power

S. Chaudhry and M. Racanelli

TowerJazz, 4321 Jamboree Rd., Newport Beach, CA 92660

Abstract- The large customer breadth of the Specialty Foundry is driving process technology and design enablement innovation that is hard to replicate within an integrated device manufacturer (IDM) which serves a more focused customer base. In this paper we will review Specialty Foundry technology in the areas of RF, high-performance analog, and power. We will also review novel design enablement tools available from the Specialty Foundry that leverage the tight interaction between EDA, models, and process technology to improve time to market and yield of highly integrated analog products.

I. INTRODUCTION

The Foundry space is split into two dominant segments: the Digital Foundry and the Specialty Foundry. The Digital Foundry leverages a large capital investment into relatively standardized technology that serves a large set of customers in a uniform way and is primarily focused on scaling CMOS. The Specialty Foundry leverages engineering service together with a more modest capital investment to serve smaller but more custom markets such as those of RF, analog, and power. In this paper we will focus on this second segment of Foundry and discuss how it has evolved to provide technology and design enablement that in many cases surpasses that available within IDMs (companies that own their own manufacturing that have more traditionally dominated specialty markets).

Specialty ICs typically have a large analog and a relatively smaller digital content (often referred to as analog-intensive-mixed-signal or “AIMS” ICs). They are critical components of state-of-the-art communication, power management, and storage systems, where analog performance is of paramount importance and where the requirements of large-scale digital integration are secondary. Unlike digital-centric designs where switching speed and power-consumption largely drive the process technology, there is almost an unlimited set of device level figures-of-merit that define the requirements on specialty process technology. These include, but are not limited to, active transistor gain, low and high frequency noise, linearity, isolation, efficiency, matching, self-heating, device on-resistance, memory access time, and resonator quality. It is apparent that “one-size” fits all technology solution is not a viable option in the specialty process technology domain.

An often overlooked consideration in evaluating foundry technology options for AIMS ICs relates to Design Automation. The demands on compact model accuracy, layout dependent parasitic extraction, and physical synthesis and verification tools, have dramatically increased for the sub-90nm digital technologies. It has, however, often been incorrectly assumed that these requirements do not apply to the analog design environments, since most AIMS designs are

at mature technology nodes. For instance, it was very common for Low Noise Amplifier (LNA) design community to add fictitious noise sources to compensate for missing “excess” noise [1] in MOSFET compact noise models. Empirical approaches such as these have prevented complete exploration of the design parameter space, resulting in sub-optimum designs at higher costs.

In this paper, a two pronged approach to mitigating the challenges of the AIMS IC design is presented. First, a Specialty Foundry process platform is described serving the needs of RF, analog, and power management IC design. Second, design-enablement tools that maximize performance and lower costs and time-to-market are presented.

II. AIMS Process Technologies

Over the last decade the technology needs of AIMS ICs have diverged from those of digital ICs. Unlike digital CMOS, performance of analog components typically does not improve with scaling and therefore innovation in analog components such as SiGe bipolars, high-voltage MOSFETs, and high-performance passives has occurred in more mature lithography nodes as shown in Figure 1.

For many AIMS applications today, the 0.18 μm node is the sweet-spot of new design activity while for digital-centric design it is moving beyond the 65nm node. In the remainder of this section, we will therefore focus on a 0.18 μm process platform, although similar technology exists to varying degrees in the 0.13 μm node.

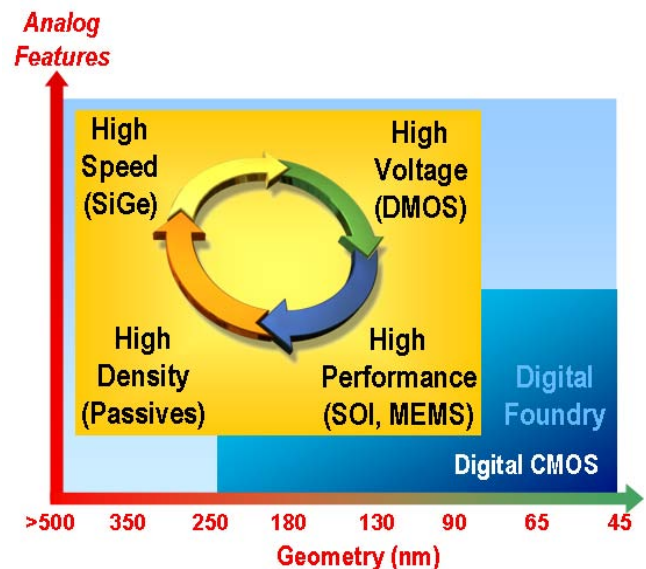


Figure 1: Scaling trends for AIMS vs. digital ICs

A. Specialty process technology platforms

Specialty Foundries offer modular platforms which augment a base technology with modular features that can satisfy a wide range of applications. In this way, a single platform can be leveraged across many markets providing a cost advantage over technology created in an IDM serving a narrower range of applications. In addition to a cost advantage, the platform concept allows Specialty Foundry customers the ease of IP re-use as IP created for one application can be re-used in another by adding or subtracting features without changing much of the base process. Figure 2 shows one such platform. All features described are modular although not all can co-exist (for example SiGe transistors are not offered on the same wafer as 40V LDMOS, but the core 0.18 μ m CMOS transistors are the same, so core IP can be leveraged in an RF and power management application). In the next two sections we will describe the state of the art performance of these modules split into two major categories: RF and High Performance Analog (HPA) Modules, and Power Modules.

NVM, MEMS	
12V LDMOS	20-40V LDMOS
Analog RF Features: PNP, PA, DSV	
200GHz SiGe	38 -155GHz SiGe
5V CMOS	3.3V CMOS
0.18 μ m CMOS (1.8V)	
SOI	

Figure 2. TowerJazz 0.18 μ m Platform serving RF, High Performance Analog, and Power Management applications through a rich set of modular features.

RF and HPA Modules: SiGe transistors are the most important RF module enabling high gain stages through higher f_T and f_{MAX} , lower noise figure, higher voltage and power handling all at lower power consumption than possible with the base 0.18 μ m CMOS. The most important applications for SiGe transistors include wireless transceivers, optical network transceivers, TV tuners, power amplifiers, and very high speed emerging applications such as automotive collision avoidance at 24 and 77GHz, 60GHz WLAN, and phased-array radar satellite receivers. Figure 3 shows state of the art f_T as a function of emitter current for a 1 μ m length transistor. Speeds of 200GHz are offered in production with 0.18 μ m transistors but speeds as high as 270GHz have been demonstrated on the same platform [2]. While f_T is only one important figure of merit, it can be traded off for lower noise, higher f_{MAX} , lower

power consumption and therefore is the most benchmarked figure of merit for SiGe bipolar transistors [3].

In addition to NPN transistors, many applications can make use of a complementary device such as a high-speed vertical Si PNP transistor. This is particularly true when “driving” a load where a push-pull output stage is desired. Figure 4 shows high speed PNP transistors demonstrated on this same platform. Standard offerings in this platform include PNP transistors with f_T of 18GHz and with BV_{CEO} of up to 14V. SiGe NPNs tailored for power amplifier (PA) applications along with deep-silicon vias (DSV) for low inductance grounds are also available [4].

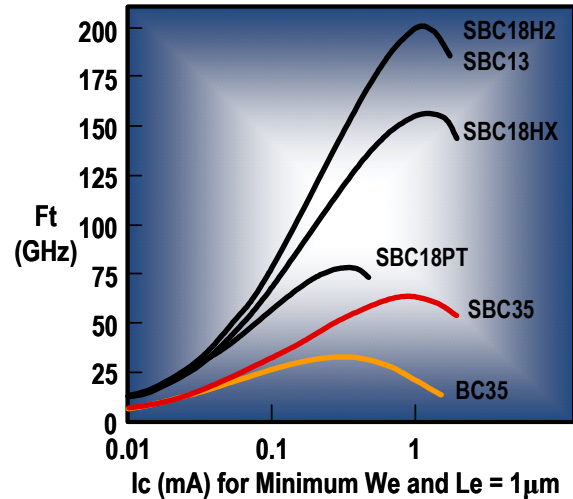


Figure 3. TowerJazz SiGe transistor performance. SBC18 transistors are available in the platform described in Figure 2.

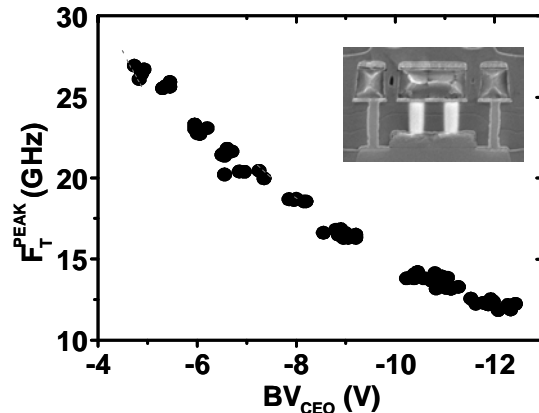


Figure 4. TowerJazz PNP transistor measurements. Transistors at 18GHz and up to 14V are available in the platform described in Figure 2.

Passive elements can be an important addition to analog and RF circuits and are standard offerings in a Specialty Foundry. State of the art inductor metal thickness is up to 6 μ m of Al or 3.3 μ m of Cu. In many cases the Specialty Foundry offers multiple thick layers of metal for building high-Q inductors, baluns and transformers, power combiners, or simply for large power handling. In addition, flexibility in

choosing the number of metal layers, allows the designer to optimize the die-size/cost trade-off.

In addition to passive elements, isolation features such as deep trenches are common. The platform depicted in Figure 2 also has an SOI option that allows building of CMOS (and experimentally SiGe transistors) with complete oxide isolation. This is very useful in RF switch applications where a large voltage is isolated by stacking multiple transistors that are allowed to “float” and distribute the voltage evenly across their terminals so as to not to exceed voltage ratings of any one transistor. Figure 5 shows measured results of a six pole RF switch built in this process as an example. The RF switch is a major component of any cell phone and WiFi front-end-module and, while traditionally built in III-V pseudomorphic High Electron Mobility Transistors (pHEMT) technology, is now enabled by Specialty Silicon Foundries by use of SOI.

IL Ant-Tx (0.9GHz)	0.6 dB
IL Ant-Tx (1.9GHz)	0.9 dB
Iso Tx-Rx (0.9GHz)	47 dB
Iso Tx-Rx (1.9GHz)	34 dB

Figure 5. TowerJazz SP6T RF Switch IP performance built in the platform described in Figure 2 showing insertion loss (IL) and Isolation (Iso) at low and high band and intended for cellular switch application.

Power Modules: Two major modules that enable many power applications are the LDMOS transistors and embedded non-volatile-memory (NVM). LDMOS transistors enable high voltage handling to co-exist with advanced CMOS logic functions while embedded NVM enable trimming and calibration code storage among other uses.

The key figure of merit of LDMOS transistors is the R_{dson} (on-resistance) as a function of voltage handling. A unique feature of the platform in Figure 2 is that it allows the entire voltage range from 20 to 40V (now also extended to 60V) to be covered by a single transistor with a scalable drain extension. In this way, each transistor in the design can be optimized in a continuous manner for minimum R_{dson} based on the voltage it needs to sustain. This feature can save significant die area in a power management IC by not forcing “overdesign” relative to voltage which often occurs when the device is not scalable in this fashion.

There are many NVM options offered by Specialty Foundries mainly from 3rd party providers. In the platform described in Figure 2, the Specialty Foundry offers its own NVM option: YFlash. YFlash is a multiple-time-programmable, single floating gate module with only a $2\mu\text{m}^2$ cell size [5] capable of being used as a compact one-time-programmable memory or a multi-time-programmable memory without requiring additional processing in the core $0.18\mu\text{m}$ CMOS technology. The MEMS capability in Figure 2, is based off advanced process modules for etch, encapsulation, and integration with the baseline AIMS processes.

III. AIMS Design Enablement

Design enablement tools, including silicon-verified device models and flexible design environments, allow IC design teams to test, modify and improve the functionality and yield of new products long before the first prototype is manufactured. The role of a specialty foundry is key in enabling a design environment that is easy to install and use, while being accurate and feature-rich to enable first-time success on silicon. In fact, customers of specialty foundries can benefit from the experience of the foundry in de-bugging and improving these tools over several hundreds of designs before them; a benefit typically not available to customers of IDM foundries. As a case study, the TowerJazz SBC18 Process Design Kit (PDK) bug report over time is shown in Figure 6, and illustrates the relative stability of the PDK.

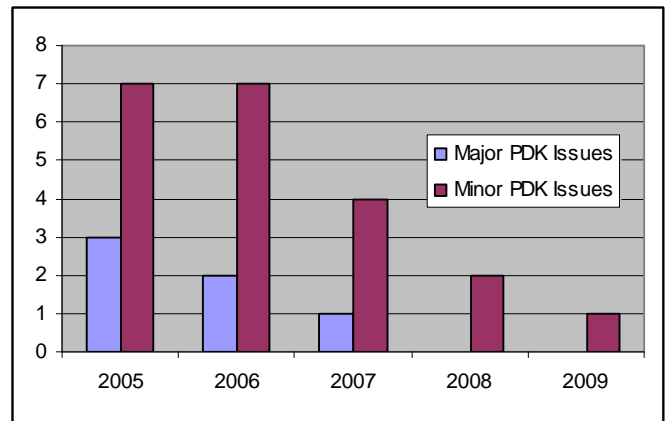


Figure 6: TowerJazz SBC18 bug-report analysis over time, showing systematic reduction in issues reported by customers.

Design enablement tools for AIMS ICs at TowerJazz can be classified into four distinct categories (Figure 7); each with its own set of goals.

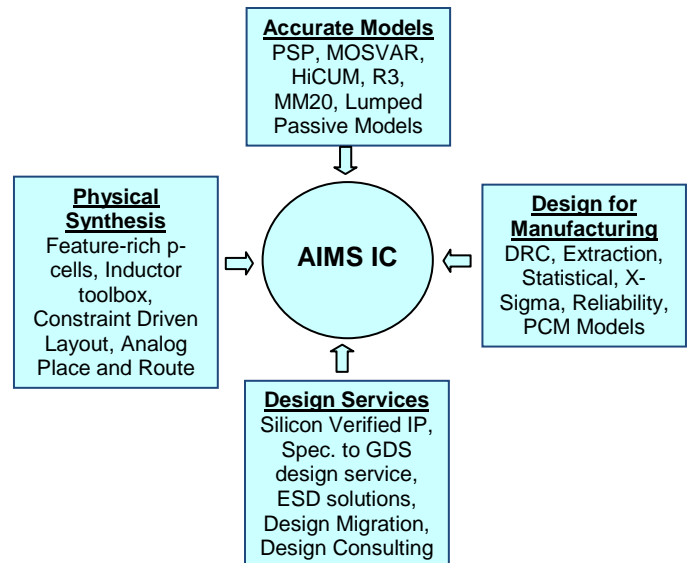


Figure 7: TowerJazz’s design enablement offering.

Front-End Modeling: The need for accurate front-end models is essential for AIMS ICs, where the performance trade-offs extend to multiple dimensions. This is in contrast to digital ICs, where optimization is typically limited to speed and power consumption. In a mobile communication system, for instance, the active devices' gain must be optimized vis-à-vis linearity, noise and power consumption. Advanced front-end models, such as PSP [6] (surface-potential based MOS Model) for MOSFETs or HICUM (HIgh CUrrent Model) for NPNs, allow for accurate modeling of active devices. For high-power applications, modeling thermal effects is critical. Advanced models such as the MM20, coupled with advanced characterization capability using pulsed systems allow accurate self-heating models to be developed for these devices. Likewise, accurate high-frequency models based off advanced 4-step de-embedding techniques [7] are essential for inductors and varactors to ensure first-time success.

Design for Parametric Yield: Process variation is inherent in any fab. Digital design has long relied on fast, typical and slow corners to evaluate the impact on a circuit's yield. These corner models typically target digital-centric figures of merit, such as speed and power consumption, and have limited use for AIMS designs where the targeted figure of merit is often not known to the modeling engineer. A statistical model, which mimics the random variation of independent process variables in a fab, is the most accurate method of simulating process variation (Figure 8). Statistical model extraction techniques, such as backward propagation of variance (BPV), allow models to align with fab process control monitoring (PCM) statistics [8]. X-sigma modeling is a sub-class of statistical models, and allows the designer to trade-off yield vs. performance by designing for 1 to 6 sigma tolerances [9].

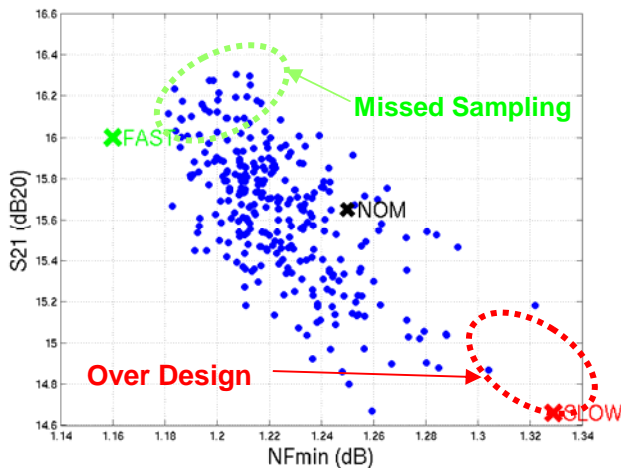


Figure 8: A monte-carlo simulation of gain (S_{21}) vs. Noise Figure of an LNA, shows regions of the device parametric space that are missed by the conventional corner models.

Physical Design Enablement: Beginning with geometry scalable and feature rich p-cells and extending to accurate extraction of layout parasitics, physical design enablement capability allows a designer to optimize a device's performance across the geometry space. Noteworthy in the

TowerJazz design enablement offering is the Inductor toolbox that allows a search capability on thousands of pre-characterized inductors. Recent advances in Electronic Design Automation (EDA) tools [10], now allow AIMS foundries to support schematic and design rule drive layout, with analog place and route capability. These tools are critical from taking a conceptual design in the schematic to tape-out stage, and are often the bottleneck in AIMS design flows.

IP and Design Services: Silicon verified digital and analog IP can be key in filling the knowledge gaps within the AIMS IC design team, while providing a quick path to large scale functional integration. Such IP could range from pre-characterized building blocks for power amplifiers, or complete solutions such as LNAs. Design centers internal to the specialty foundry allow it to offer turnkey "specification to GDS" services to the AIMS customer. They also provide valuable and rapid feedback to the process technology developers and CAD engineers within the specialty foundry, often identifying issues long before customers have access to the process technology or PDKs.

IV. CONCLUSION

It has been shown that the Specialty Foundry is driving process technology and design enablement innovation that is hard to replicate within an integrated device manufacturer (IDM), which serves a more focused customer base. As a case-stude, we have reviewed a modular, 0.18 μ m Specialty Foundry platform serving RF, high-performance analog, and power IC design. We also reviewed novel design enablement tools created by Specialty Foundries that leverage the tight interaction between EDA, models, and process technology to improve time to market and yield of highly integrated analog products.

V. REFERENCES

1. C. H. Chen and M. J. Deen, "High frequency noise of MOSFET's. I. Modeling," *Solid-State Electron.*, vol. 42, pp. 2069–2081, Nov. 1998
2. Edward Preisler et al., 2008 BCTM.
3. M. Racanelli et al., 2004 TED Special Issue on RF Technology.
4. V. Blaschke et al., "A Deep Silicon Via (DSV) Ground for SiGe Power Amplifiers," *SiRF 2010*.
5. YFlash manual, TowerJazz.
6. G. Gildenblat, et al., "PSP: An Advanced Surface-potential-based MOSFET Model for Circuit Simulation Electron Devices," *IEEE Transactions*, Vol. 53, Issue 9, September 2006, pp. 1979–1993.
7. T.E. Kolding, "A Four-Step Method for De-Embedding Gigahertz On-Wafer CMOS Measurements," *IEEE Trans. Electron Devices*, vol. 47, no. 4, Apr. 2000
8. C.C. McAndrew, "Statistical Modeling for Circuit Simulation," *Quality Electronic Design*, 2003 Proceedings, Fourth International Symposium, March 2003, pp. 357–362.
9. J. Corodovez et al., "Design Enablement for RF and Microwave IC Design: Part II," *Microwave Journal*, January 2008.
10. IC6.1 product brief, www.cadence.com