Scaling and application of commercial, feature-rich, modular mixed-signal technology platforms for large format ROICs

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ABSTRACT

Today's modular, mixed-signal CMOS process platforms are excellent choices for manufacturing of highly integrated, large-format read out integrated circuits (ROICs). Platform features, that can be used for both cooled and un-cooled ROIC applications, can include (1) quality passives such as 4fFμm^2 stacked MIM capacitors for linearity and higher density capacitance per pixel, 1kOhm high-value poly-silicon resistors, 2.8μm thick metals for efficient power distribution and reduced I-R drop; (2) analog active devices such as low noise single gate 3.3V, and 1.8V/3.3V or 1.8V/5V dual gate configurations, 40V LDMOS FETs, and NPN and PNP devices, deep n-well for substrate isolation for analog blocks and digital logic; (3) tools to assist the circuit designer such as models for cryogenic temperatures, CAD assistance for metal density uniformity determination, statistical, X-sigma and PCM-based models for corner validation and to simulate design sensitivity, and (4) sub-field stitching for large die. The TowerJazz platform of technology for 0.50μm, 0.25μm and 0.18μm CMOS nodes, with features as described above, is described in detail in this paper.

KEYWORDS

ROIC, focal plane arrays, MIM capacitor, LDMOS, NPN, PNP, deep n-well, cryogenic models, large die, stitching

1. INTRODUCTION

Read out integrated circuit (ROIC) designs are mixed signal as they comprise of both analog and digital building blocks. As pixel sizes shrink in ROICs, there is an increasing requirement to add more functionality and minimize power consumption for both cooled[1,2,3,4] and uncooled[5,6,7] applications. The integration of mixed-signal/analog specialty commercial wafer foundry offerings, which include high performance passive devices (MIM capacitors, resistors, thick top metal for inductors), various active devices (e.g., native FETs, NPNs, PNPs, LDMOS devices), isolation schemes and combinations of features from different CMOS nodes, are available in today's specialty foundry.

First, we will detail the process technology platforms at TowerJazz that could be used for ROICs or focal plane arrays. The available process technologies range from the 0.5μm technology node to the 0.18μm technology node. The feature rich modular mixed-signal 0.18μm CMOS platform could become the technology of choice for next generation large format ROICs as it could enable migration to higher pixel density, smaller pixel sizes, low power consumption, and high functional integration.

Second, we will describe design enablement features from the TowerJazz mixed-signal technology platforms. They include linear high density MIM capacitors, low noise transistors, cryogenic models, statistical and X-sigma models, local metal and poly density evaluation tools, and stitching for large format designs.

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2. PROCESS TECHNOLOGY PLATFORMS

In this section, we will describe the 5V C05H, CP05 and BCD25 process technology platforms, 3.3V only CA25 process technology platform, and dual gate oxide 1.8/3.3V as well as 1.8V/5V CA18 process technology platforms which have been developed for commercial digital, mixed-signal, analog and power products and which can be used for ROICs.

2.1 C05H/CP05 process technology platform

Earlier generation ROICs have been traditionally built on 5V platform for both cooled and uncooled applications. These ROICs have been built in 1µm or larger geometries, and extend down to 0.5µm process technology nodes. In addition to existing products in 0.5µm process node, as older fabs running larger geometry process nodes close or shut down process lines, there is a trend to migrate these earlier generation ROICs to longer life and low cost 0.5µm CMOS process node. In this section we describe a couple of low cost process technologies using single gate oxide 5V only CMOS at TowerJazz. Table 1 shows a summary of the C05H and CP05 0.5µm process technologies.

The C05H process technology node offers 5V FETs in a 0.5µm mixed signal CMOS process which includes a linear TM to poly capacitor (0.59fF/µm^2 density, < 30ppm/V linear voltage coefficient and < 20 ppm/V^2 quadratic voltage coefficient), unsilicided precision n-poly resistors and nwell resistors as well as parasitic vertical pnp device with moderate beta.

The CP05 process technology node is an enhanced version of the C05H process with optimized 5V FETs having low on-resistance of 4.1 mohm-mm^2 and 10.3 mohm-mm^2 for N- and P-channel devices, respectively, to achieve high power transistors occupying very small die area for use in low-dropout regulators, amplifiers, drivers, and other power management functions for commercial applications. However, the other features in the CP05 process technology, such as a 0.25µm process technology aluminum backend metallization which enables denser metal routing, 2fF/µm^2 high density linear MIM capacitors and high value 1kOhm/sq precision unsilicided p-poly resistors, makes it an attractive choice for low cost but enhanced 5V large die ROIC designs.

Process			**C05H**	**CP05**	**Units**
CMOS	**Vdd**		5	5	V
	5V NMOS	Vt	0.67	0.67	V
		Idsat	0.52	0.52	mA/µm
		Gate L	0.6	0.6	µm
	5V PMOS	Vt	0.83	0.83	V
		Idsat	0.26	0.26	mA/µm
		Gate L	0.6	0.6	µm
	Metal 1 pitch		1.2	***0.64***	µm
	Metal layers		3	3	
Resistor	**Nwell**		1K	1K	ohm/sq
	Poly (low value)		110	110	ohm/sq
Capacitor	**TM/Poly**		0.59		fF/µm^2
	MIM			2	fF/µm^2
Bipolar	**VPNP parasitic**	Beta	15	15	
Isolation			LOCOS	LOCOS	

Table 1: Features of C05 and CP05 process technology platforms.

2.2 BCD25 process technology platform

The BCD25 process technology platform is a high voltage CMOS process that consists of 5V CMOS devices (non-isolated), 5V CMOS devices (isolated with ability to float to > 50V with respect to substrate), 10V drain-extended nFETs (isolated and non-isolated), 8V drain-extended pFETs, 20-40V non-isolated drain-extended nFETs (with breakdown to > 50V), 25V isolated drain-extended nFETs, 20-40V drain-extended pFETs, low threshold voltage native nFETs, high value and low value unsilicided poly resistors, nwell resistors, high density linear 2fF/μm^2 MIM capacitor, high-beta VNPN bipolar transistor, VPNP bipolar transistor, schottky diode, native FETs and triple well isolation using deep n-well. The BCD25 process technology is used in complex power management applications, driver ICs, battery and portable power management for many consumer, communications and computing applications. The availability of a five layer metal 0.25μm node backend, high density 2fF/μm^2 MIM capacitors, high performance bipolar NPN and PNP, deep n-well isolations and ability to handle voltages higher than 5V makes the BCD25 process technology platform a good low cost option.

Process			BCD25	Units
CMOS	Vdd		5	V
	5V NMOS	Vt	0.67	V
		Idsat	0.48	mA/μm
		Gate L	0.6	μm
	5V PMOS	Vt	0.86	V
		Idsat	0.26	mA/μm
		Gate L	0.6	μm
	Metal 1 pitch		0.9	μm
	Metal layers		5	
Resistor	Nwell		530	ohm/sq
	Poly (low value)		100	ohm/sq
	Poly (high value)		920	ohm/sq
Capacitor	MIM		2	fF/μm^2
Triple Well Isolation			yes	
Bipolar*				
Isolation			LOCOS	

* See separate table

(a)

			BCD25			
			NFET		PFET	
Vgs	Vds	Isolated	Rdson (mohm-mm^2)	BVdss (V)	Rdson (mohm-mm^2)	BVdss (V)
5V	5V	Y	3.4	>8	10.8	>8
5V	8-12V	Y	19.6	>14	42.5	>14
5V	20V	Y	26	>26	75	>35
5V	40V	N	62	>48	175	>50
5V	40V	Y	84	>42	175	>50

(b)

	BCD25		
	NPN	HV NPN	PNP
Beta	11.5	130	10
VA (V)	300	26	82
BVceo (V)	>16	>13	>12
Bvcbo (V)	>35	>42	>42

(c)

Table 2: Features of BCD25 process technology platform (a) general devices (b) LDMOS devices and (c) bipolar devices

2.3 CA25 process technology platform

The CA25 process technology platform is a mixed-signal CMOS process that consists of 3.3V CMOS devices with shallow trench isolation. It is the last generation of single gate process, where both nFET and pFET has n+ doped poly gates. The pFETs are buried channel devices due to the counter-doped nwell required for reasonable threshold voltage. The flicker noise for buried channel pFET is significantly less than the surface channel FETs in smaller geometry process technology nodes. The availability of low 1/f noise pFETs, high density linear 2fF/μm^2 MIM capacitors, dense 0.25μm CMOS node backend metallization pitch, unsilicided poly resistors, nwell resistors, and parasitic vertical pnp in the commercial CA25 process technology platform can be used for many ROIC applications. Cryogenic models, up to 78K, are also available for this process along with optional 12V Vds drain-extended FETs. It may be noted that as CMOS process geometries scaled down, the CA25 is the first process node to use shallow trench isolation (STI) instead of local oxidation of silicon (LOCOS) isolation.

Process			**CA25**	**Units**
CMOS	**Vdd**		3.3	V
	3.3V NMOS	Vt	0.59	V
		Idsat	0.55	mA/μm
		Gate L	0.36	μm
	3.3V PMOS	Vt	0.74	V
		Idsat	0.3	mA/μm
		Gate L	0.36	μm
	Metal 1 pitch		0.64	μm
	Metal layers		4	
Resistor	**Nwell**		1200	ohm/sq
	Poly (low value)		92	ohm/sq
Capacitor	**MIM**		1, 2	fF/μm^2
Bipolar	**VPNP Parasitic**	Beta	4	
Isolation			STI	

Table 3: Features for CA25 process technology platform

2.4 CA18 process technology platform

The CA18 process technology platform supports 1.8V digital CMOS as well as its mixed-signal, analog and RF variants with 26Å (physically measured) pure gate oxide and 0.18μm minimum drawn gate length. CA18HD has a dual gate oxide process which includes the 26Å gate described above, and transistors for interfacing to circuits up to 3.3V nominal with 57Å (physically measured) thick pure gate oxide. This digital/mixed-signal/RF process has six layers of aluminum metal. It supports unsilicided high value (1kOhm/sq) and low value (310kOhm/sq) poly resistors, 2fF/μm^2 density MIM capacitor, 4fF/μm^2 density stacked MIM capacitors, low threshold voltage native nFETs, parasitic vertical pnp, triple well isolation using deep n-well and 2.8um thick top metal 6 for inductors in an RF CMOS process. Cryogenic models down to 78K are available for this process variant. The CA18HA process is another dual gate oxide process for interfacing to circuits up to 5V nominal with 130Å (physically measured) thick pure gate oxide transistors. In comparison to CA18HD, the CA18HA process has the 3.3V FETs replaced by the 5V FETs, while preserving the other active and passive devices of the CA18HD process. A summary of the CMOS parameters for these two processes is made in Table 4. In addition, the 1.8V/5V dual gate oxide CA18HA process has 5V CMOS devices (non-isolated), 5V CMOS devices (isolated with ability to float to > 50V with respect to substrate), 12V drain-extended NFETs (isolated and non-isolated), 12V drain-extended PFETs, 20-40V non-isolated drain-extended NFETs (with breakdown to > 50V), 20-40V isolated drain-extended NFETs, 20-40V drain-extended pFETs and high voltage npn bipolar device (see Table 5).[8] The scalable drain-extended devices can be used for ROICs designed for various high voltage detector applications. The available bipolar devices can be used for low noise biasing applications as well as in precision band gap voltage reference circuits. The 1kOhm/sq high value unsilicided poly resistors can be used for quenching circuits, resistive trans-impedance amplifiers (RTIA) as well as digital to analog converters. The triple well isolation using deep n-well allows a convenient substrate isolation scheme for individual devices and circuit blocks as well as body biasing. Many of these elements for RF, mixed signal, analog and power applications are also attractive for ROIC applications.

Process			CA18 - 3.3V	CA18 - 5V	Units
CMOS	Vdd		3.3	5	V
	3.3V NMOS	Vt	0.62	-	V
		Idsat	0.6	-	mA/μm
		Gate L	0.36	-	μm
	3.3V PMOS	Vt	0.74	-	V
		Idsat	0.25	-	mA/μm
		Gate L	0.3	-	μm
	5V NMOS	Vt	-	0.65	V
		Idsat	-	0.52	mA/μm
		Gate L	-	0.6	μm
	5V PMOS	Vt	-	0.77	V
		Idsat	-	0.26	mA/μm
		Gate L	-	0.6	μm
	1.8V NMOS	Vt	0.52	0.52	V
		Idsat	0.6	0.6	mA/μm
		Gate L	0.18	0.18	μm
	1.8V PMOS	Vt	0.44	0.44	V
		Idsat	0.26	0.26	mA/μm
		Gate L	0.18	0.18	μm
	Metal 1 pitch		0.64	0.64	μm
	Metal layers		6	6	
Resistor	Nwell		890	890	ohm/sq
	Poly (low value)		310	310	ohm/sq
	Poly (high value)		1000	1000	
Capacitor	MIM		2,4	2,4	fF/μm^2
Triple Well Isolation			yes	yes	
Isolation			STI	STI	

Table 4: Features for CA18 process technology platform (CMOS parameters)

	CA18HA					
	Vgs (V)	Vds (V)	Vt (V)	Rdson (mohm-mm^2)	BVDSS (V)	IDSAT (mA/μm)
High Voltage NLDMOS	5	20	0.68	21.5	>25	0.3
	5	40	0.68	50	>45	0.3
Isolated High Voltage NLDMOS	5	20	0.68	27	30	0.3
	5	40	0.68	64	43	0.3
High Voltage PLDMOS	5	20	0.88	79	>25	0.14
	5	40	0.88	169	>45	0.14

	CA18HA HV NPN
Beta	112
Early Voltage	24.5V
Bvceo	>11V
Bvebo	>7V
Bvcbo	>36V

Table 5: Features for CA18HA process (drain-extended FET and bipolar npn parameters)

The 2.8µm thick top aluminum metal module available in the above mentioned TowerJazz CA18 processes is beneficial for large die applications as it allows efficient power distribution and low I-R drops across the large die. The schematic shown in Fig. 1 shows the thick top metallization scheme. Optional 5.2µm thick aluminum metallization is also available. The design rule pitch for the thick top metal layer is 4.5µm for both 2.8µm and 5.2µm thick aluminum metallizations, enabling integration of compact high Q inductors for RF applications.

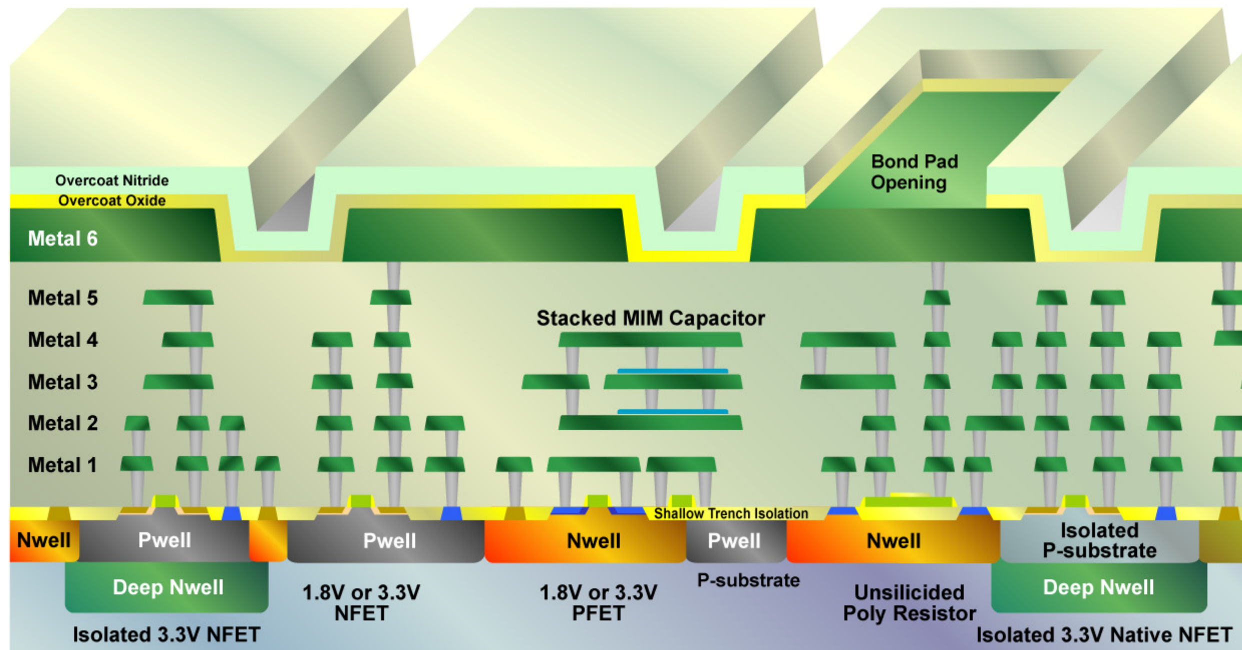


Fig. 1: Schematic cross-section of a 1.8/3.3V CA18 process technology node

3. DESIGN ENABLEMENT FEATURES

The modularity of TowerJazz high performance devices enables porting of those devices between different technology nodes to create hybrid processes, These hybrid processes can, for example, enable high levels of integration as well as good performance in noise and power. In this section, we discuss in more detail some of the TowerJazz active and passive devices and design enablement features available in multiple process technology nodes.

3.1 High density linear MIM capacitors

As in many high performance mixed-signal, analog, RF and power products, ROICs can require integrated high density MIM capacitors. The MIM capacitors available at TowerJazz have low voltage and temperature coefficients, good capacitor matching, precision control of capacitor values and low parasitic capacitance along with high reliability and low defect density. Tower Jazz offers high density 2fF/µm^2 MIM capacitors[9,10] consisting of a bottom metal plate (Metal 2 for example), a thin PECVD nitride dielectric layer, and an intermediate TiN conductor plate connected to the metal layer above (Metal 3 in this example). The capacitor can be stacked to form 4fF/µm^2 with another 2fF/µm^2 MIM capacitor consisting of the same metal 3 as the bottom plate, another thin PECVD nitride dielectric layer and another intermediate TiN conductor plate connected to the Metal 4 layer above. The Metal 2 and Metal 4 are electrically connected together to form one node of the stacked parallel capacitors and the Metal 3 layer provides the connectivity to the other capacitor node. The stacked parallel capacitor configuration also advantageously cancels out the already low linear voltage coefficient in single layer MIM capacitors. Table 6 summarizes the properties of these MIM capacitors. These MIM capacitors have excellent matching for single layer MIM as well as the stacked MIM capacitors. Typical

capacitor mismatch results are shown in Fig. 2. Common centroid MIM capacitor layout configurations can be used to further improve capacitor matching than that shown in Fig. 2. Higher stacked MIM capacitor density of 5.6fF/μm^2, comprising of two 2.8fF/μm^2 high density MIM capacitors with scaled down PECVD nitride dielectric, is available in newer process technology variants. These MIM capacitors can also be stacked with the poly to substrate MOS capacitors for even higher capacitor densities.

Description	Nominal Value		Units
	2fF/μm^2 MIM capacitor	4fF/μm^2 stacked MIM capacitor	
Area Capacitance	2.0	4.0	fF/μm^2
Perimeter Capacitance	0.23	0.6	fF/μm
Linear Voltage Coefficient (LVCC)	-40	0	ppm/V
Quadratic Voltage Coefficient (QVCC)	25	25	ppm/V^2
Temperature Coefficient	20	20	ppm/°C

Table 6: Specifications of the 2fF/μm^2 MIM capacitor and 4fF/μm^2 stacked MIM capacitor

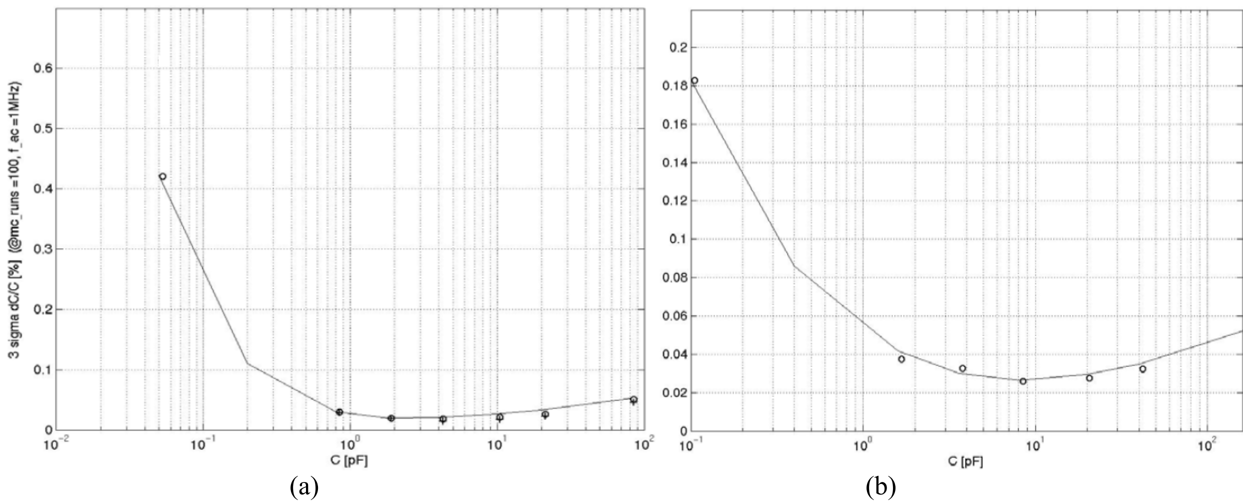


Fig. 2: Capacitor matching data for (a) 2fF/μm^2 MIM capacitor and (b) 4fF/μm^2 MIM capacitor

3.2 Low noise FETs

Buried channel FETs are preferred for low noise designs because of inherent low 1/f noise of the buried channel. Fig. 3 shows the 1/f noise reductions obtained in the buried channel 3.3V pFETs versus a surface channel 3.3V pFET. This makes the CA25 process technology node popular for low 1/f noise applications. There is currently development activity in the CA18 node for buried channel devices.

In addition, all TowerJazz technology nodes described here, including the CA18 process technology node, have pure gate oxide instead of nitrided gate oxide. The nitridation within the gate stack introduces charge traps thereby resulting in higher low frequency noise versus pure gate oxides.

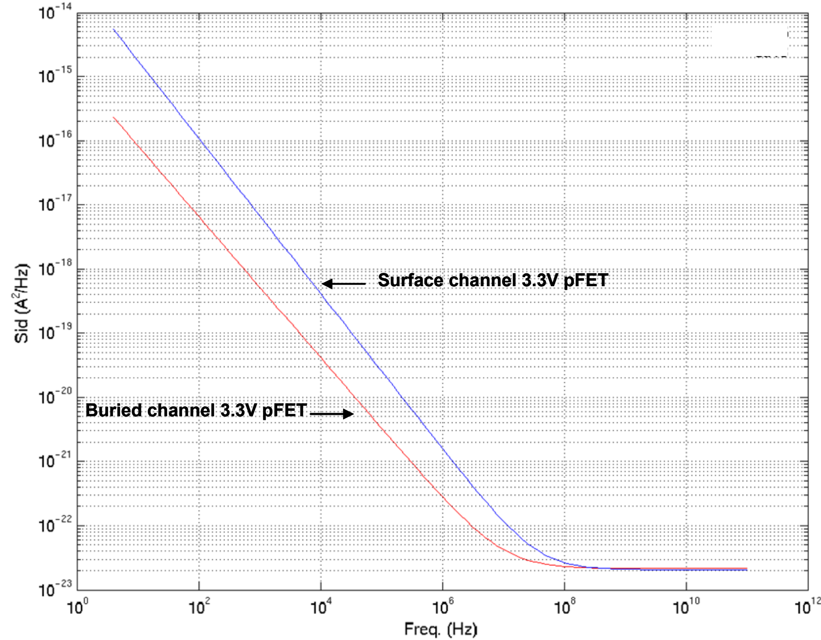


Fig. 3: 1/f noise comparison between buried channel and surface channel 3.3V pFETs

3.3 Cryogenic models

TowerJazz offers models for FETs operating at cryogenic temperatures. Fig. 4 shows the model playbacks for 1.8V nFETs operating at room temperature (298K) and at cryogenic temperature 78K. The key advantage of FETs operating at cryogenic temperatures is greater than 2x improvement in low field mobility even with higher threshold voltages. The use of low Vt native nFETs operating at cryogenic temperatures can yield reasonable threshold voltages with improved mobilities. Silicon verified cryogenic models are currently available at TowerJazz for the CA25 and CA18 process technology nodes.

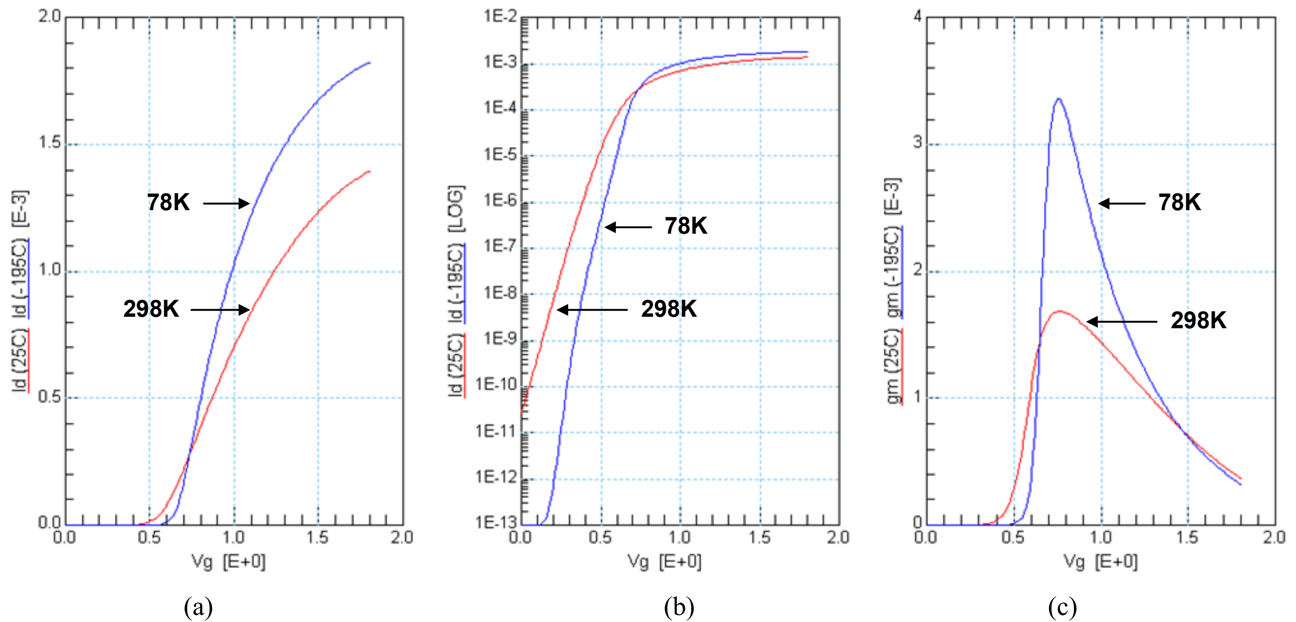


Fig. 4: Model playbacks for 1.8V nFET (WxL = 10x0.18um) at 298K (room temperature) and 78K in linear regime for (a) I_{drain} versus V_g (b) I_{drain} versus V_g (subthreshold (c) gm

3.4 Local density of conductor layers

Multi-level aluminum metallization processes with silicon dioxide as the interlayer layer dielectric (ILD) employ subtractive etch for patterning of metal and poly-silicon layers and chemical mechanical planarization (CMP) to planarize the interlayer dielectric before patterning the subsequent via and metallization layers. Metal fills are added to low metal density layers to satisfy minimum global metal density requirements. However, during the planarization step by CMP, the oxide on top of metal lines in regions with sparse metals and narrow metal lines, get polished at the fastest rate and large regions with dense wide metals or large metal plates get polished at the slowest rate. This is a characteristic of the CMP removal process resulting in potentially large local topography variations within a die. In multi-metallization processes, the local topography for each layer could be cumulative and cause larger local topography variations in upper metallization layers, negating some of the benefits of the planarization process (See Fig. 5). The local topography variation causes local focus offsets during the photolithography process. This narrows the photolithography process window, and can cause yield loss or create defect issues. To address low metal fill areas, metal fill can be drawn in the metal layer design to assist the CMP process for local and global planarization of the ILD.

TowerJazz has developed a graphic user interface tool to generate the local conductor densities for each individual conductor layers (poly, metals) as well as stacked conductor densities. Fig. 6 shows an example of the local metal density of a metal layer obtained before and after metal fill. In the example shown, the metal 3 density varies from less than 10% to higher than 50% before metal fill. After metal fill, the minimum metal densities are close to 40% for most of the chip area. During gds data submission to foundry, local conductor density plots are reviewed as part of data acceptance. Smart metal fill techniques must be employed to ensure local metal density uniformity and improved CMP planarization for stacked conductor densities to prevent large intra die topography variations.

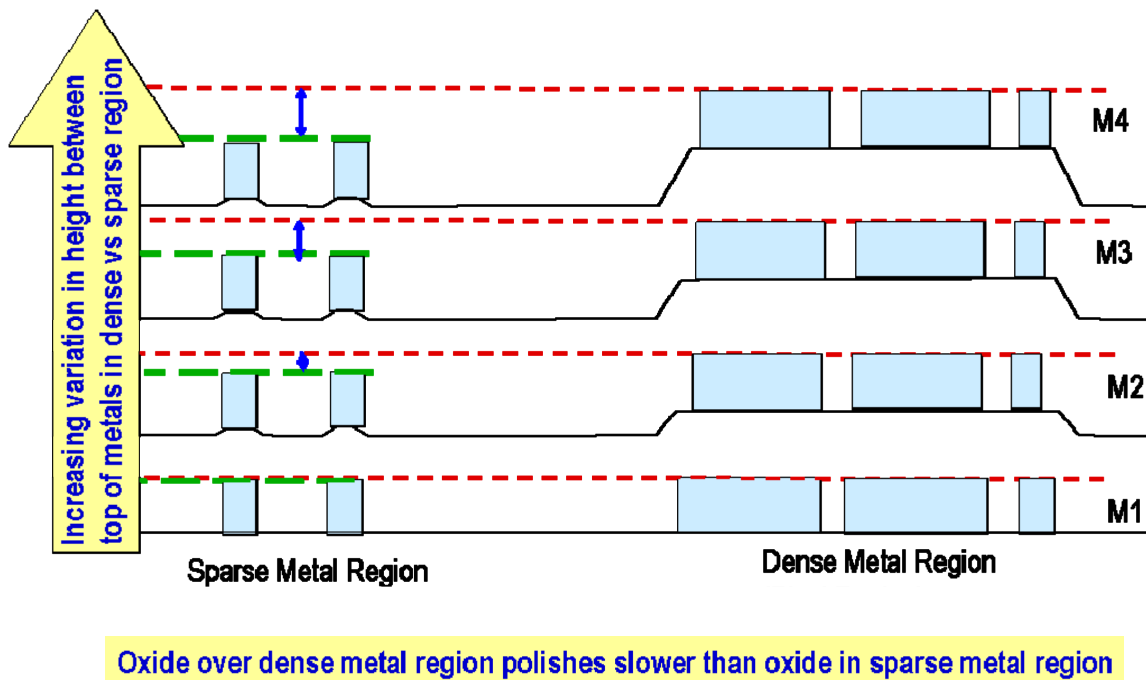
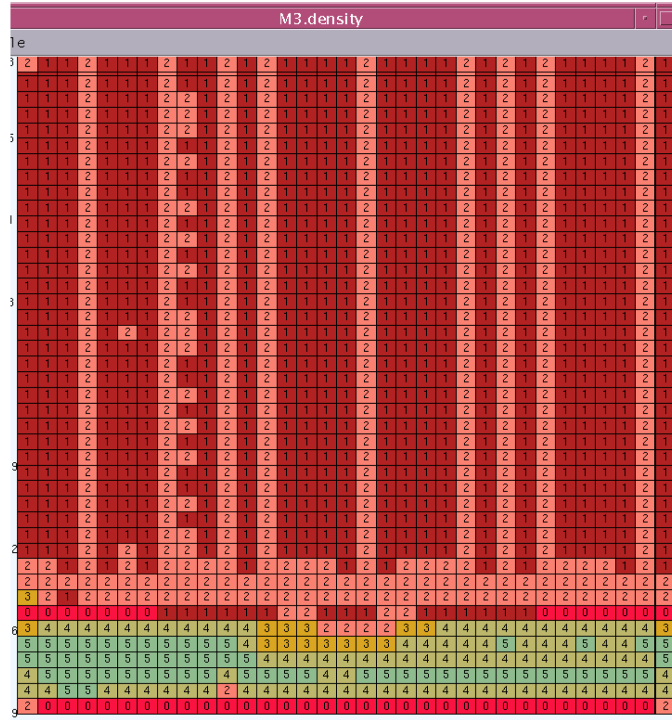
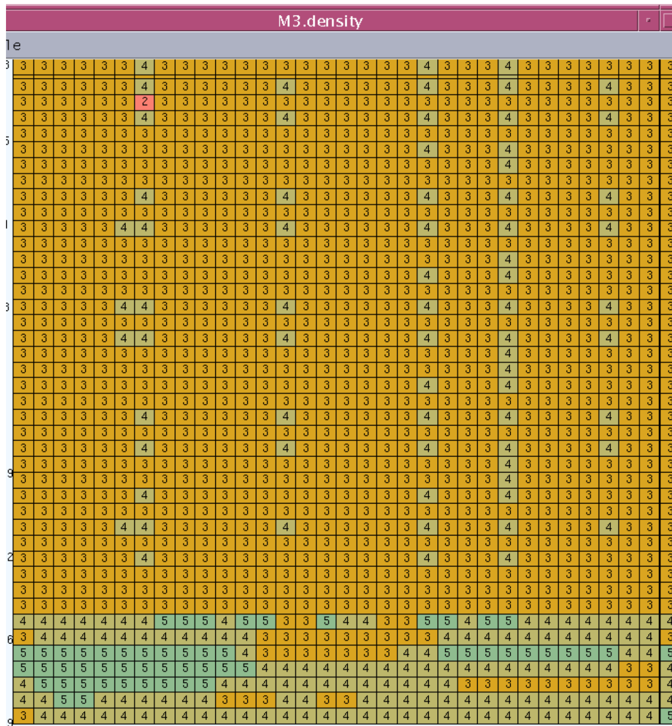


Fig. 5: Schematic illustrating topography variations over regions of dense and sparse metal density. Note that the topography variations are not to scale and are exaggerated for illustration purposes.



(a)



(b)

Fig. 6: Example of local metal density uniformity TowerJazz GUI tool outputs for (a) before metal fill (b) after metal fill. The density for local windows (typically 400μm x 400μm) is displayed and the density numbers are binned as 0% < 0 <10%, 10% < 1 < 20%, 20% < 2 < 30%, and so on.

3.5 Statistical, X-sigma and PCM-based models

TowerJazz uses a physical approach to model extraction using advanced compact models such as PSP and HiCUM or internal verilog-A based models. This allows models to be accurate and scalable across a wide range of geometries, thereby giving the user the flexibility to trade-off performance for size. Based on this scalable modeling platform, a backward propagation technique[11] is used to generate statistical models to evaluate design sensitivities. A subset of the statistical modeling platform is the X-sigma tool, which allows the user to trade-off performance with parametric yield. Post-silicon design sensitivity analysis is enabled via an innovative PCMT tool,[12] that enables automated generation of PCM-based (process control monitoring) models valid for the die/wafer that the chip was diced from. Recently, an innovative Reliability Modeling Tool (RMT) has been developed to enable designers to simulate the impact of operating bias and age on integrated circuits.

3.6 Stitching

One commercially available method to create die sizes larger than allowed reticle field size is to fabricate and singulate multiple smaller die which fits individually within the reticle fields and then mosaic them together into the large array using edge buttable packaging techniques.[13] This may require multiple masksets and complex packaging techniques, while potentially leaving dead row and column regions in the final product. In another method called reticle stitching, the large die design is partitioned into multiple design blocks smaller than the reticle field. Multiple reticle exposures are then made per layer to re-compose the entire large die extents on the wafer. The stitched boundary regions of the small design blocks get double or multiple exposures and are accounted for in the design. The reticle stitching method becomes more expensive as the die size increases and as the process technology node shrinks because of the high cost of multiple reticle sets.

Another method, called sub-field stitching, is the preferred choice for die sizes greater than the reticle field for designs with repeating blocks. In the preliminary design phase, the design has to be first partitioned into multiple design blocks some of which are repetitive. The next step consists of the placement of the unique design blocks in the reticle as sub-fields separated by a minimum distance required by the photolithography tool to blade off each subfield. Finally, imaging of the unique design blocks to re-compose the full die on a wafer has to be verified with the process foundry. A close working relationship must be maintained between the design team and the process foundry during the design phase of subfield stitched large area designs to verify that the assumptions of the partitioning of the design are actually manufacturable without any systematic yield loss. During photolithographic exposure in sub-field stitched designs, the subfields are double exposed in the overlap regions. TowerJazz has stitched design rules to account for the double or multiple exposures in the overlap regions, as well as misalignments, magnification and rotational errors with the photolithography equipment. The overlap regions are typically less than 0.5um.

Die sizes as large as the wafer size can be built using a single reticle set. Tower Jazz has manufactured die sizes as large as 5-inch x 6-inch in commercial production using sub-field stitching.[14]

4. CONCLUSIONS

In conclusion, the commercial, feature-rich TowerJazz process technology platforms, which span across 0.5µm to 0.18µm CMOS process nodes, have features that may be highly applicable for use in ROIC applications. These process technology platforms include the C05H, CP05, BCD25, CA25, and dual gate oxide 1.8/3.3V CA18 and 1.8V/5V CA18 processes. The availability of quality active and passive devices such as high density linear stacked 4fF/μm^2 MIM capacitors, high value precision poly resistors, low noise NPN bipolars, parasitic vertical PNPs, high voltage LDMOS devices, buried channel pFETs, low threshold voltage native FETs, triple well isolation using deep n-wells for substrate isolation schemes and FET body biasing, and 2.8µm and thicker metallization across different process platforms were described. Design enabling statistical, X-sigma and PCM-based models as well as silicon verified cryogenic models, have potential for cooled ROIC applications, and were described. Sub-field stitching and local metal and poly density tools for large format designs are available for most process technology platforms.

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