

# A 1.6–3.2-GHz Sixth-Order + 13.1-dBm OIP3 Linear Phase $g_m$ - $C$ Filter for Fiber-Optic EDC Receivers

Dalius Baranauskas, Denis Zelenin, Matthias Bussmann, Salam Elahmadi, Jomo K. Edwards, and Christopher A. Gill

**Abstract**—A sixth-order low-pass  $g_m$ - $C$  filter for fiber-optic electrical dispersion compensation receivers cascades three bi-quads permitting a reduction of group delay variation down to 10 ps. A cutoff frequency is tuned from 1.6 to 3.2 GHz by using two methods, namely, changing  $g_m$  and switching a CMOS varactor's polarity. Output third-order intercept point reaches 13.1 dBm and total harmonic distortion is below  $-40$  dB at  $0.9 V_{pp-diff}$  output. The continuous time filter is implemented in a  $0.18\text{-}\mu\text{m}$  SiGe process, it occupies  $0.17\text{ mm}^2$  on a  $3.2 \times 3.7\text{ mm}^2$  test chip and consumes  $0.3\text{ W}$  from a  $3.3\text{-V}$  supply.

**Index Terms**—Active filter, antialiasing filter, continuous time filter (CTF),  $g_m$ - $C$  filter, high-speed integrated circuit, optical fiber dispersion compensation.

## I. INTRODUCTION

A CONTINUOUS time filter (CTF) is a critical block of wireline, wireless, and, more recently, fiber-optic systems [1]. As the data rates are growing high-order gigahertz bandwidth (BW) low-pass filters are increasingly demanded in DVD and hard disk read channels. Antialiasing filters applied in front of digitizers are needed for ultra wideband and software defined radios. An analog implementation of electrical dispersion compensation (EDC) in adaptive fiber-optic receivers requires a low-pass fourth–sixth-order 1.8–2.5-GHz BW range CTF featuring linear phase (see Fig. 1). Higher order gigahertz range filters are currently limited to  $LC$ -based implementation [2], [3].  $g_m$ - $C$ , also known as an operational transconductance amplifier capacitor (OTA- $C$ ), is one of the most popular active filter techniques offering the tuning ability and occupying a small on-chip area. However, this technique is normally used in the MHz range [4], [5]. This paper presents a small form factor  $g_m$ - $C$ -based CTF with the cutoff frequency tunable from 1.6 to 3.2 GHz, a linear phase response, high-output third-order intercept point (OIP3) and a wide dynamic range. Some of the features of this filter are presented in [6].

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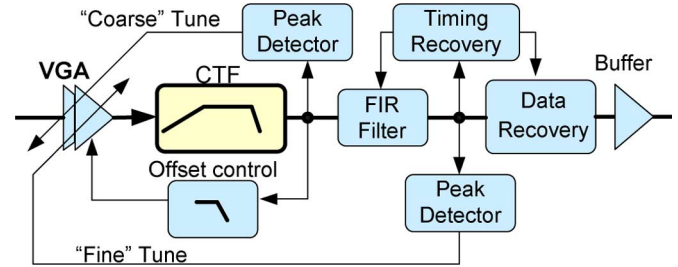


Fig. 1. Block diagram of an analog EDC receiver.

This paper introduces new data on reference current generation circuits for filter biasing, the test chip's output buffer design and presents the circuits for filter input signal normalization, namely, gain and offset control. The aspects of physical implementation of this filter are discussed by presenting the layouts of the critical blocks. In addition, new measurement data are presented, the CTF is compared with existing similar designs. Section II explains in detail the CTF's architecture. Section III shows the I/Os—voltage-to-current ( $V2I$ ) and current-to-voltage ( $I2V$ ) converter designs. Sections IV and V present the OTA circuit and the CTF's BW tuning aspects. Sections VI and VII describe the CTF's input signal normalization and current reference circuits. Section VIII introduces the physical implementation of the CTF. Section IX presents and discusses the experimental results. Finally, in Section X, conclusions and findings are presented.

## II. ARCHITECTURE

The proposed sixth-order CTF cascades three bi-quads (see Fig. 2). The transfer characteristic of one biquad is [9]

$$H(s) = \frac{g_m V2I g_m2}{C_1 C_2 s^2 + (g_m3 C_1 + g_m C_2) s + (g_m1 g_m2 + g_m3 g_m C)}$$

where  $g_m1, g_m2, g_m3, g_m V2I$ , and  $g_m C$  are the transconductances of OTA1, OTA2, OTA3,  $V2I$ , and  $Q_c$ , respectively. Biquad cascading requires that  $H(0) = g_m V2I g_m2 / (g_m1 g_m2 + g_m3 g_m C) = 1$ . This ensures that the biquads are operating at the same signal level, which is necessary for simpler cascading. Assuming that  $g_m C = 0$ , we have  $H(0) = 1$  when  $g_m V2I = g_m1$ . By rearranging  $H(s)$  to the normalized form:  $H(s) = K / (s^2 + \beta s + \gamma)$ , we have,  $\beta = g_m3 / C_2$  and  $\gamma = g_m1 g_m2 / C_1 C_2$ . In order for the filter performance to remain unchanged over the technology parameter corners, the filter quality factor  $Q = \sqrt{\gamma} / \beta$  should not depend on either  $g_m$  or capacitance, which will be used for the cutoff frequency tuning. Assuming that  $C_1 = C_2 = C$

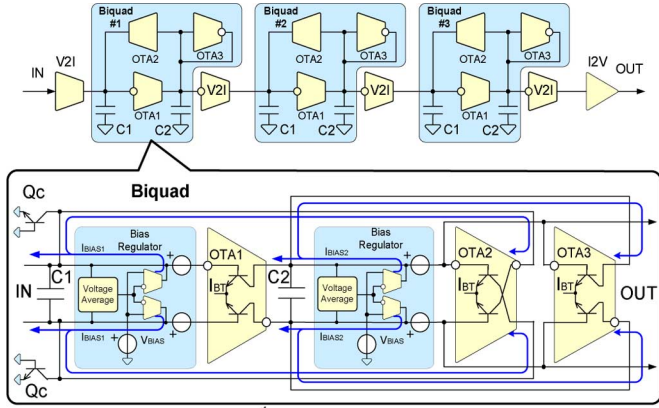


Fig. 2. Block diagram of the sixth-order CTF consisting of three biquads and the implementation of a differential biquad.

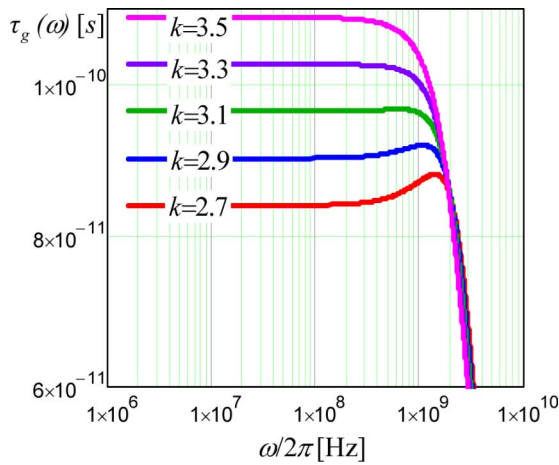


Fig. 3. Simulated filter group delay over frequency.

and  $g_{m1} = kg_{m2} = kg_m$ , we obtain  $Q = \sqrt{k}/k$ . As follows from  $\omega_{0p} = \sqrt{\gamma} = g_m\sqrt{k}/C$ , the filter pole frequency  $\omega_{0p}$  can be tuned by changing the value of  $g_m$  and  $C$ . Filter phase response over frequency is characterized by the group delay  $\tau_g = (-d)/(d\omega)\varphi(\omega)$ , where  $\varphi(\omega) = \arg(H(\omega))$ . Group delay for different  $k$  is simulated by means of Mathcad and results are presented in Fig. 3. As can be seen, the best group delay performance is achieved when  $k = 3.1$ . For this reason, we are setting the transconductances of the CTF OTAs as  $g_{m1} = g_{m3} = kg_{m2} = kg_{V2I}$ , where  $k = 3.1$ .

Cascading three biquads reduces the CTF's BW  $\sqrt{3}$  times. The resulting group delay of the three biquads is  $\tau_{g2}(\omega) = 3 \times \tau_g(\omega)$ . The horizontal group delay region remains flat. As a result, the CTF's group delay horizontal region extends further with respect to CTF's BW. A frequency response of a single biquad and cascaded CTF was simulated by means of Mathcad (see Fig. 4).  $\Delta\tau_{g1}$  is the change of a single-biquad group delay when frequency reaches the BW point (see Fig. 4).  $\Delta\tau_{g2}$  and  $\Delta\tau_{g3}$  shows the change of the CTF group delay to the BW point and to the  $1.3 \times$  BW point, respectively.  $\Delta\tau_{g1}$  is much larger compared to  $\Delta\tau_{g2}$  and is almost the same as  $\Delta\tau_{g3}$ . This result proves the merit of our methodology for reducing the CTF's group delay variation.

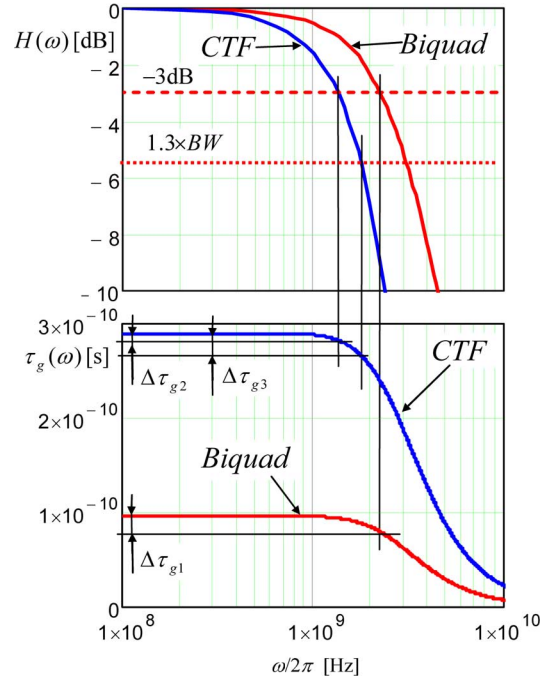


Fig. 4. Single-biquad and three-biquad-based CTF transfer characteristics and group delay response.

In order to obtain a CTF cutoff frequency of 3.2 GHz, the biquad's cutoff frequency has to be about 5.5 GHz. The inter-stage  $V2I$  converters'  $g_m$  has to be set the same as that of OTA2  $g_m$  in order for the biquad to have 0-dB dc gain. Biquads are implemented as fully differential circuits in order to increase the power supply rejection ratio and the common mode rejection ratio. OTA3 response is equivalent to resistance equal to  $1/g_m$ . Despite the possibility of power saving, the replacement of OTA3 by a resistor would lead to the increase in the CTF's parameter variation over process corners.

The  $C_1$  connection node is loaded by one OTA input, while  $C_2$  is loaded by three OTA inputs, causing the node capacitance ratio (ideally 1:1) to vary over process corners and temperature. Level shifters (implemented as emitter followers) provide higher voltage for the OTA's transistor collectors and help isolate the OTA's parasitic loading. Residual loading mismatch is compensated by a circuit represented by  $Q_c$ . The OTA bias currents  $I_{BIAS1}$  and  $I_{BIAS2}$  are generated by a circuit that sets the average output voltage at  $V_{BIAS}$ .

### III. I/O BUFFERS

The CTF's buffers are designed in such a way as to have their cutoff frequencies exceeding those of the biquads in order to minimize the impact on the CTF's performance. The CTF input  $V2I$  converter is based on the Cherry–Hooper amplifier (see Fig. 5) [7] featuring linearity as well as high speed. The output current is delivered by the diff-pair ( $Q_7, Q_8$ ), which replicates  $Q_3, Q_4$  as well as the  $V2I$  converters used between biquads. The CTF's output  $I2V$  buffer (see Fig. 6) is based on the same Cherry–Hooper configuration. Load resistor  $RL$  is split to pull up the amplifier input bias voltage in order for the last  $V2I$



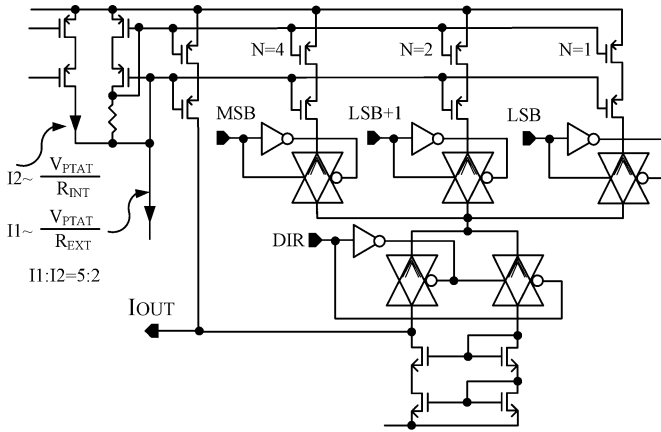
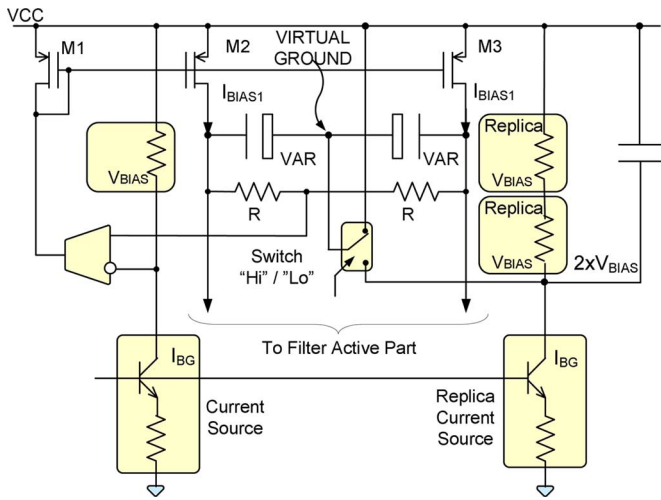

 Fig. 10. 3-bit plus “sign” binary coded DAC used for  $g_m$  programming.


Fig. 11. Varactor biasing circuit.

The PTAT reference compensates  $g_m$  temperature dependency, while  $R_{EXT}$  makes  $g_m$  insensitive to the on-chip resistance. The remaining secondary effect of the on-chip resistance on the cutoff frequency is compensated by subtracting the part of the current set by  $R_{INT}$ . The resulting current in OTAs is slightly increasing when the internal resistance increases. The current variation by the DAC is limited to a relatively small  $\pm 25\%$  range since  $g_m$  tuning also results in the change of linearity, biasing points and dynamics of OTAs. For this reason, capacitance programming is the preferred method for tuning the cutoff frequency. MIM or MOS capacitors connected in series with the CMOS switches is a commonly used method. The combination of the capacitance with the resistance of the switch in ON and OFF states deteriorates the capacitor's quality ( $Q_c$ ) and produces unwanted time constants. We propose to use the MOS varactors instead of switched capacitors. The backside of the varactor is switched between  $+1.25$ - and  $-1.25$ -V bias with respect to the gate (see Fig. 11). It changes the capacitance by about three times according to Fig. 12 (based on actual data provided by the silicon foundry for  $\pm 3\sigma$  process corners). Most importantly, the backside connection point of the varactors is a virtual ground in a differential circuit. The parasitics introduced to this point by the switches have negligible effect on the CTF's

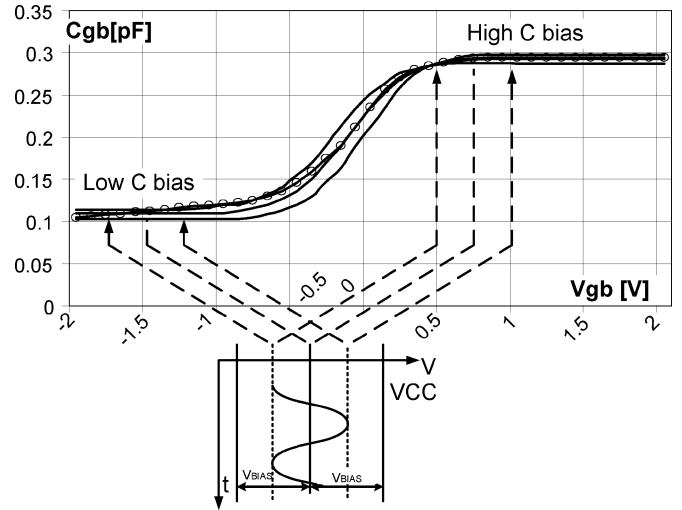


Fig. 12. Varactor tuning curve.

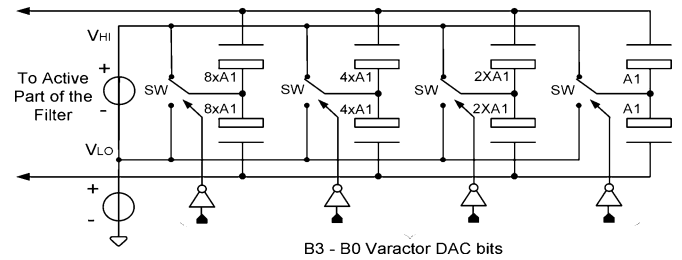


Fig. 13. Varactor tuning DAC.

performance. In order to minimize the capacitance modulation by the signal, the biasing points are set on the flat portions of  $C(V)$  diagram (see Fig. 12). The varactor backside can be switched between  $V_{CC}$  and  $2V_{BIAS}$ , while the gate remains at  $V_{BIAS}$  (see Fig. 11).

The varactors are scaled as 1:2:4:8 and are combined into a 4-bit DAC (see Fig. 13). The implementation of a dual cutoff frequency control allows the use of  $g_m$  tuning (considering its impact on other CTF's parameters) for fine adjustment only.

## VI. CTF INPUT SIGNAL NORMALIZATION

A linear variable gain amplifier (VGA) (see Fig. 14) is implemented as a part of a dual-loop automatic gain control (AGC) that adjusts the signal amplitude at the CTF output (coarse loop) and at the finite-impulse response filter output (fine loop) (see Fig. 1). The AGC compensates for the VGA output signal level change caused by the input signal variation and VGA circuit gain variation caused by the variation of temperature and the power supply voltage. The overall gain (from  $-19.5$  to  $+20.5$  dB) is controlled by a current from a two 7-bit DACs. The first DAC is responsible for coarse control (from  $-16$  to  $0$  dB) and the second DAC is responsible for the fine control (from  $-12$  to  $0$  dB). The DACs are controlled by an AGC state machine with the capability to overwrite the control through a serial peripheral interface (SPI) control register. In order to ensure monotonic transfer characteristics aiming to avoid the AGC loop malfunction, thermometer coding is used in the DACs. AGC loops maintain a  $900\text{-mV}_{pp\text{-diff}}$  swing data signal.

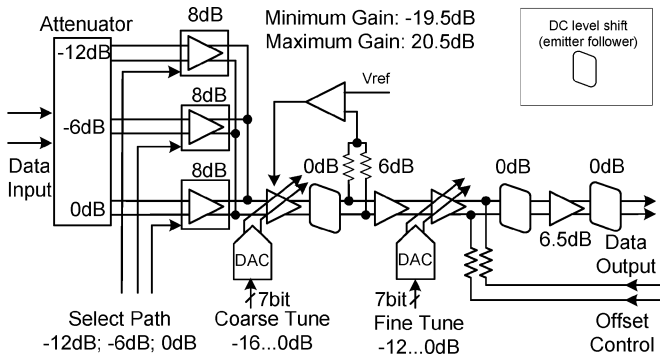


Fig. 14. Simplified VGA block diagram.

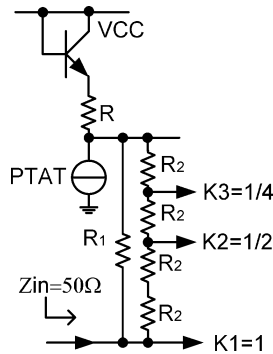


Fig. 15. Simplified (only single-ended signal path shown) schematic diagram of the attenuator.

at the CTF output. This corresponds to about  $250 \text{ mV}_{pp-diff}$  at the CTF input.

To provide stepped attenuation, a programmable attenuator is built in with  $-12$ -,  $-6$ -, and  $0$ -dB attenuation steps for accommodation of the large dynamic range of the incoming signal. The attenuator (see Fig. 15) also includes the biasing and the  $50\text{-}\Omega$  termination functions. Resistors  $R_2$  form the resistive divider, which provides transfer coefficients of  $1$ ,  $1/2$ , and  $1/4$ . Since sheet resistance of the used resistors is  $235 \text{ }\Omega/\text{square}$ , the resistor  $R_1$  is connected in parallel with the divider to make it possible to increase the resistance of  $R_2$ . This helps reduce the divider's resistor area and, subsequently, the parasitic capacitance resulting in improved  $S_{11}$ .

The automatic offset control block (see Fig. 16) cancels out any offset in the signal chain along the CTF and the last gain block ( $6.5 \text{ dB}$ ) in the VGA. To avoid offset control loop BW and, subsequently, the CTF's low frequency cutoff variation depending on the VGA gain, the variable gain part of the VGA is not enclosed in the offset control loop. Instead of an  $RC$  filter, a  $g_m$ - $C$ -based loop filter is used for setting the low frequency response of the automatic offset control. The implementation of the  $g_m$  cell requires much less on-chip area compared to megohms of resistance necessary for the low cutoff frequency for the  $RC$  filter. Subsequently,  $1\text{-kHz}$  low-frequency cutoff is achieved. The second  $g_m$  cell is employed to convert the offset control voltage on the capacitor to the current, which is inserted into the output termination point of the last variable gain stage in the VGA.

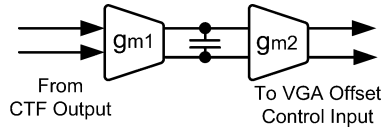
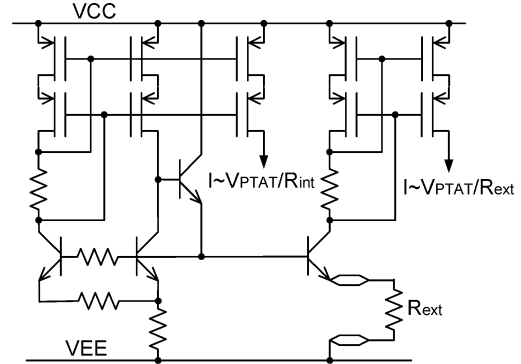


Fig. 16. Simplified offset control circuit.

Fig. 17. Schematics of the current reference block producing PTAT currents proportional to  $1/R_{int}$  and  $1/R_{ext}$ .

## VII. CURRENT REFERENCE CIRCUITS

In general, on-chip resistance may vary over process corners more than  $25\%$ , while  $g_m$  can be set virtually independent on process corners and temperature. For this reason, it is preferable to rely on  $g_m$  rather than on resistance when setting the cutoff frequency in the offset control circuit and, more importantly, in the OTAs used in the CTF. Temperature dependence of  $g_m$ , as discussed in Section V, is eliminated by using the PTAT bias current. The schematic diagram of the PTAT reference producing currents proportional to both  $1/R_{int}$  and  $1/R_{ext}$  is shown in Fig. 17.

To establish the constant over temperature bias voltage, the bandgap current reference generating current proportional to  $1/R_{int}$  has to be employed since the bias voltages are setup by passing the current through internal resistors. The bandgap current reference circuit used in this design is shown in Fig. 18.

## VIII. LAYOUT AND FABRICATION

The CTF's layout (see Fig. 19) is made as compact as possible along the direction of the signal path aiming to reduce the capacitive and resistive parasitics on sensitive high-speed signal nodes. Control and biasing circuits are moved away from the signal path and are laid out less tightly. In order to ensure the ratioed diff-pair is well balanced, particular attention is paid to its layout design. Due to the fact that there are  $12$  signal transistors and four current sources, the layout of the cell is relatively large. Consequently, it is evident that the regular symmetrical layout would space the components apart, thus compromising the symmetry in case of the process parameters and temperature gradients. To avoid this effect, the transistors in the diff-pairs are interdigitated and placed in two rows (see Fig. 20). The current source transistors and resistors are placed at the edges of the layout, namely,  $I_{E11}$ ,  $I_{E22}$  are located on one side and  $I_{E12}$ ,  $I_{E21}$  are placed on the other.

A  $0.18\text{-}\mu\text{m}$  SiGe process from Jazz Semiconductor is used for the CTF's implementation. The die size is  $3.2 \times 3.7 \text{ mm}^2$  (see

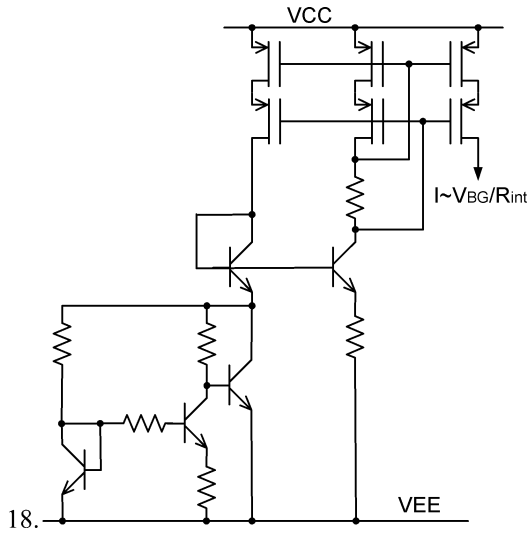


Fig. 18. Schematic diagram of the current reference block producing the bandgap current proportional to  $1/R_{int}$ .

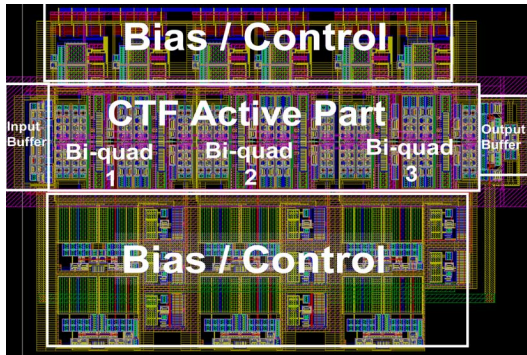


Fig. 19. CTF layout.

Fig. 21) with the CTF occupying the space of only  $0.17 \text{ mm}^2$ . The test chip is wire bonded in a custom solder bumped package. Before being delivered to the CTF, the signal on the test chip is normalized and has its offset corrected by the VGA. The CTF output signal is buffered and delivered over 1 mm distance to a  $50\text{-}\Omega$  terminated linear output buffer driving output pads through  $50\text{-}\Omega$  coplanar transmission lines. The SPI is used for the test chip configuration and tuning of the CTF's BW. The rest of the chip area is used for other functions (beyond the scope of this paper) as well as for biasing blocks and power-supply bypassing capacitors.

### IX. EXPERIMENTAL RESULTS

Before the CTF testing, the quality of the high frequency I/Os of the test chip along with the signal traces on the test board were evaluated by measuring  $S_{11}$  and  $S_{22}$ . A VNA was used for frequency response measurements. Both  $S_{11}$  and  $S_{22}$  (see Figs. 22 and 23) are reasonable over frequency range from 500 MHz to 5.5 GHz.

As a result of a dc blocking capacitor inserted in the signal path,  $S_{22}$  is deteriorating at lower frequencies ( $<500 \text{ MHz}$ ), as can be seen in Fig. 23. Next, the CTF's BW programming range was measured. Having used both varactor and  $g_m$  tuning, it was determined that the total BW tuning range was from 1.6 to

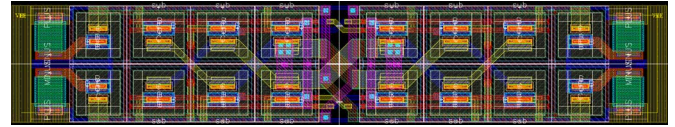


Fig. 20. Layout of the linearized OTA cell.

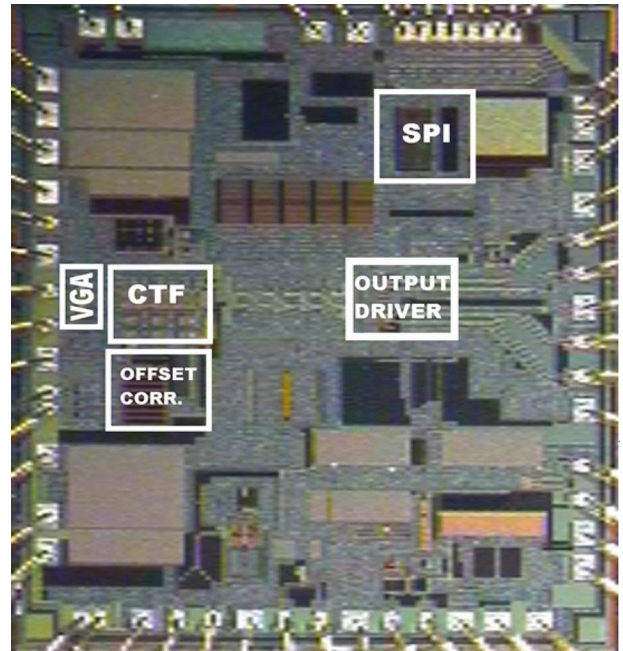


Fig. 21. CTF test chip photograph showing the main blocks.

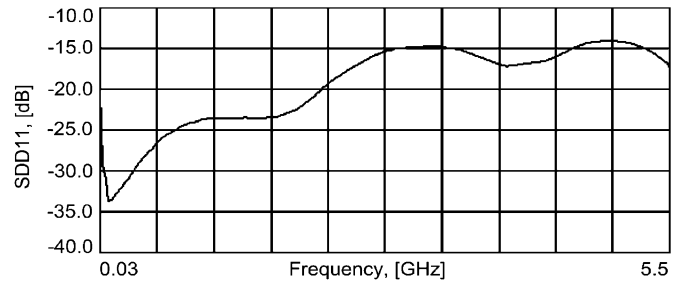


Fig. 22.  $S_{DD11}$  measured from 300 MHz to 5.5 GHz. Worst case reflections are below  $-13 \text{ dB}$ .

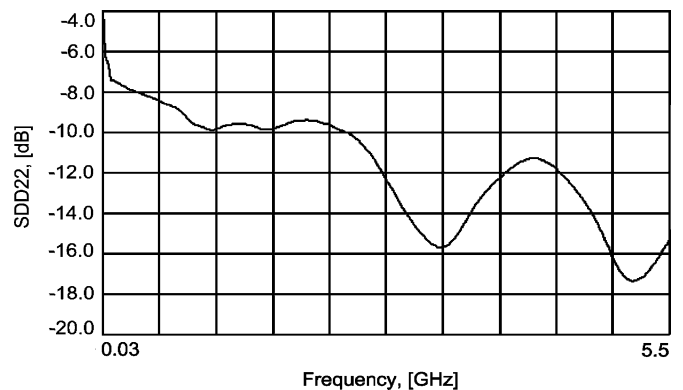


Fig. 23.  $S_{DD22}$  for the test chip output, showing reasonable reflections from about 500 MHz. High reflections at low frequencies are caused by a dc blocking capacitor.

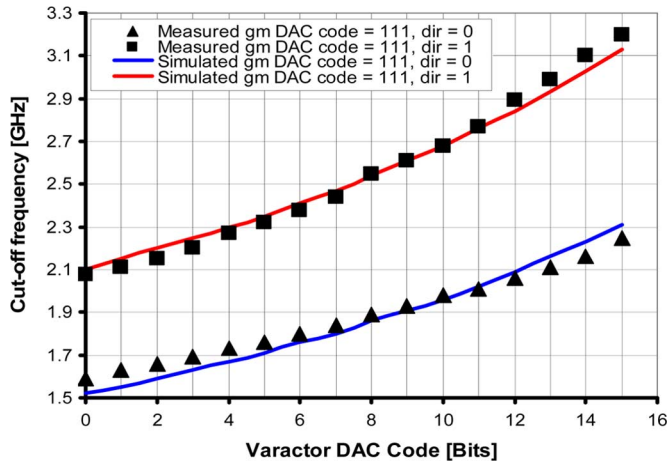


Fig. 24. Measured versus simulated BW over capacitor DAC code.

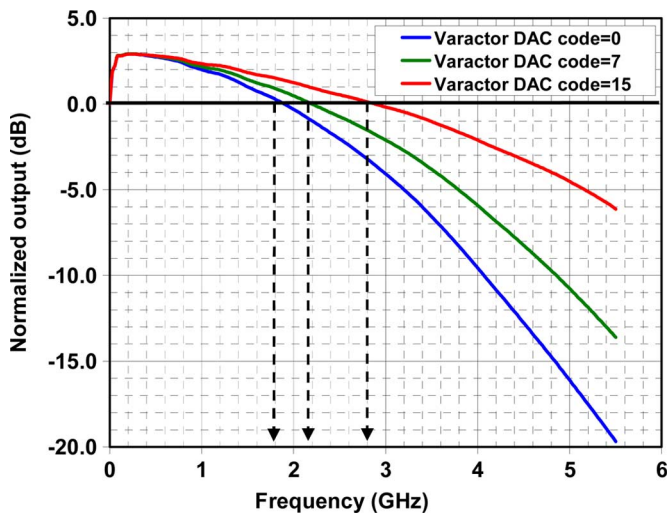


Fig. 25. Normalized CTF transfer characteristic.

3.2 GHz (see Fig. 24). The measured data closely corresponds to the data obtained in simulation by means of Spectre simulator. Minor mismatches are attributed to the limited accuracy of the component models.

The tuning varactor's capacitance alone changes the BW from 2.1 to 3.2 GHz in case when  $g_m$  DAC code set to "111" and tune direction bit is set to "1." The BW range is 1.6 to 2.2 GHz when  $g_m$  DAC code is set to "111" and tune direction bit is set to "0." The possibility of covering the frequency range from 1.8 to 2.5 GHz without using the  $g_m$  tuning is also shown (see Fig. 25). For the purposes of this measurement,  $g_m$  is adjusted to its optimum value required for covering of the targeted BW range.

The group delay change is measured to be less than 10 ps in the frequency range from 0.3 GHz up to the cutoff frequency point (see Fig. 26). The remaining group delay variation with frequency is small enough not to cause any significant visual distortion when comparing ideal, simulated, and measured eye diagrams at the CTF's output (applied 10-Gb/s nonreturn to zero (NRZ) data to the input) (see Fig. 27).

Measured total harmonic distortion (THD) at 900-mV<sub>pp-diff</sub> output (250-mV<sub>pp-diff</sub> input) voltage is below -40 dB. Measured OIP3 is 13.1 dBm. Low THD and high OIP3 justify

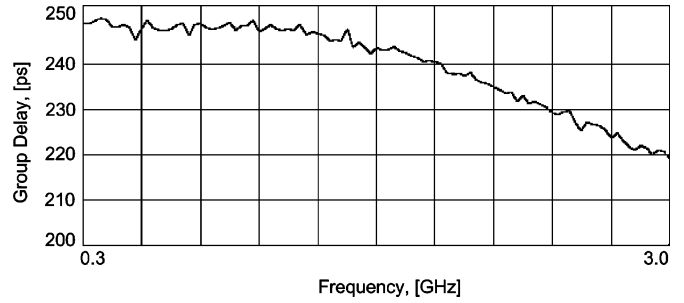


Fig. 26. CTF group delay over frequency.

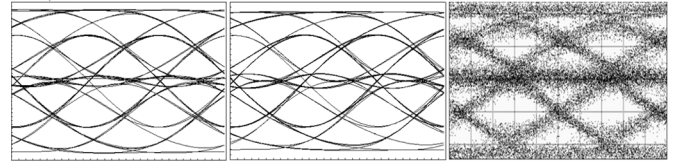


Fig. 27. CTF output response for 10-Gb/s NRZ input data: ideal filter (left), simulated schematics (middle), measured (right).

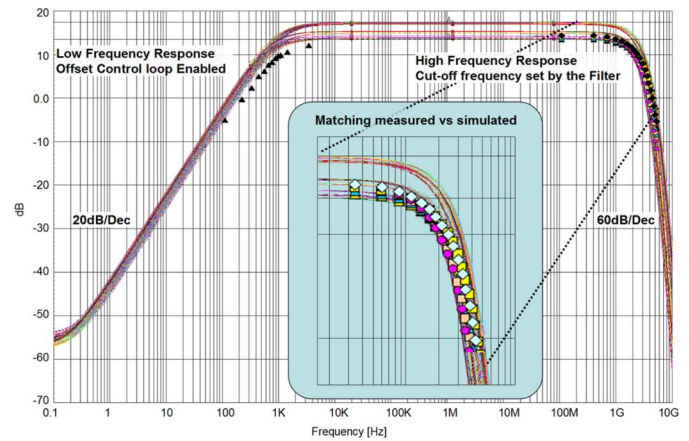


Fig. 28. CTF transfer characteristics: measured versus simulated.

the relatively high power dissipation (300 mW without output buffer). The CTF's transfer characteristics simulated for different process corners ( $\pm 3\sigma$  process corner combinations are used), power supply ( $\pm 5\%$ ), and temperature (0 °C, 125 °C) are shown in Fig. 28. Measured data points are placed on critical areas of the graph. They closely match the simulations (multiple devices were measured to obtain these data points). The low-frequency cutoff point at around 1 kHz with 20-dB slope is a result of the offset control function. Measurement data are summarized in Table I.

A comparison of this CTF with similar published designs is presented in Table II. Compared to the filters in [3] and [5], this filter reaches much higher BW. The filter presented in [8] has 4.1-GHz BW compared to our 3.2 GHz. However, our design does not require fast p-n-p transistors and is implemented in a standard SiGe process, which means that it can be powered from generic 3.3-V power supply compared to 3.5 V reported in [8]. On-chip area needed for our CTF is much smaller compared to other high frequency CTFs [3] and [8]. Higher power dissipation in our design allows us to achieve much higher OIP3. It has to be noted that the linear phase response (flat group delay) over frequency has been achieved. Most importantly, there was no

TABLE I  
PERFORMANCE SUMMARY

Process	0.18 $\mu$ m SiGe	
Group delay variation (0.1GHz-BW)	10ps	
Area	Filter	0.17mm <sup>2</sup>
	Test chip	11.84 mm <sup>2</sup>
BW tuning range	Overall	1.6 to 3.2GHz
	Varactor only (for specific gm)	1.8 to 2.5GHz
OIP3	+13.1dBm	
THD at 900mV <sub>pp-diff</sub> output	-40dB	
Power supply voltage	3.3V	
Power dissipation	300mW	

TABLE II  
COMPARISON WITH SIMILAR PUBLISHED DESIGNS

Ref.	BW [GHz]	Order	VCC [V]	Power [mW]	Area [mm <sup>2</sup> ]	Process	OIP3 [dBm]
[3]	1.1	5	1.8	72	1.38	0.18 $\mu$ m CMOS	–
[8]	0.05–4.1	5	3.5	100	0.82	0.25 $\mu$ m C-SiGe	-12
[5]	0.28	6	1.2	0.12	0.018	0.13 $\mu$ m CMOS	0
This work	1.6–3.2	6	3.3	300	0.17	0.18 $\mu$ m SiGe	+13.1

need to use on-chip resistors for the purposes of linearization or gm setting in OTAs, thus offering the stability of CTF's parameters in production.

## X. CONCLUSION

A sixth-order  $g_m$ -C continuous time linear phase (10 ps group delay variation), 13.1-dBm OIP3 filter is implemented based on the design techniques offering filter parameter stability over process corners and temperature. The achieved THD at 900-mV<sub>pp-diff</sub> output is below -40 dB. Wide BW tuning range covers frequencies from 1.8 to 3.2 GHz. Capacitance-based tuning allows the preservation of all other parameters of the filter while changing the BW within 1.8–2.5-GHz range necessary for the EDC type receivers to cover 10 to 11.3-Gb/s data rates.

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