

A 3-20 GHz SiGe HBT Ultra-Wideband LNA with Gain and Return Loss Control for Multiband Wireless Applications

Duane C. Howard, John Poh, Tonmoy S. Mukerjee, and John D. Cressler

School of Electrical and Computer Engineering

777 Atlantic Drive, N.W., Georgia Institute of Technology, Atlanta, GA 30332-0250, USA

E-mail: dhoward3@gatech.edu

Abstract—We present an ultra-wideband, low power, Low Noise Amplifier (LNA) implemented in Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT) technology. This SiGe LNA is broadband, covering the frequency range of 3-20 GHz, and achieves a peak gain of 21.3 dB. The SiGe LNA exhibits a Noise Figure (NF) of 4.3-5.2 dB across an 8-18 GHz band and consumes 35.2 mA from a 3.3 V supply.

Index Terms— BiCMOS, UWB, LNA, noise figure, SiGe, wideband.

I. INTRODUCTION

Recent advancements in silicon-based electronics technology have enabled the unprecedented growth in narrowband wireless communications that we see today. However, there has also been a growing interest in wideband systems, in particular for scientific and military applications. Wideband wireless communications systems such as ultra-wideband (UWB), nominally from 3-10 GHz, are attractive because the wide bandwidth enables higher data rates while minimizing power consumption and complexity requirements. Wideband systems also show promise in the areas of medical imaging, vehicular communications, and other short-range communications needs. In addition, C-Band (4-8 GHz) and X-Band (8-12 GHz), in particular, are actively exploited for satellite communications and a wide variety of radar systems. Thus, wireless transceivers which can simultaneously cover multiple frequency bands are extremely attractive because they potentially enable more efficient spectrum utilization.

A central component of any wireless transceiver system is the LNA, and for wideband systems the design of the LNA presents significant challenges, because they simultaneously must achieve broadband impedance matching as well as very low noise figure across the band, all at low power dissipation.

Another issue of significant importance to wireless circuits is product yield. Circuit yield can be considered to be the ratio of working circuits to the number of circuits produced. Additionally, process yield encompasses die-to-die and within-die variations, and can be caused by several factors which create faults in the manufacturing process [1]. In particular, for sensitive scientific and military applications it is especially important that circuits such as the LNA operate within specifications. Therefore, there is an emerging critical need for the development of so-called “self-healing” wideband circuits [2].

Many approaches have been offered for the design of wideband LNAs. For example, the widest bandwidth has been achieved using distributed topologies [3]. However, distributed amplifiers typically take up substantial die area and

also suffer from high noise figure (NF). Other approaches, such as common gate [4] and ladder-matched LNAs [5], also suffer from high NF. Additional approaches include staggered compensation [6] and transformer feedback techniques [7]. Both can be used to successfully extend bandwidth, but both suffer from high NF. In addition, shunt-resistive feedback has been used with some success [8]. The LNA presented here utilizes emitter degeneration, resistive feedback, and inductive peaking to increase bandwidth. A novel varactor-controlled method for the adjustment of input return loss has been developed and included. Additionally, a novel pFET gain control method is presented.

SiGe technology has become increasingly attractive for analog, mixed-signal, and RF applications because of its excellent performance and noise characteristics at conservative lithographic nodes, as well as its compatibility with existing low-cost silicon-based processes. The present wideband LNA was implemented in the commercially-available 0.18 μm , 150 GHz f_T Jazz Semiconductor (SBC-18) SiGe HBT BiCMOS process technology.

II. CIRCUIT ANALYSIS AND DESIGN

The LNA is a three stage design. The schematic of the SiGe LNA is shown in Fig. 1. The LNA has a common-emitter (CE) input, with emitter resistive and capacitive degeneration. The capacitive degeneration is implemented by using a varactor which can be biased to tune the capacitive load and adjust the input matching as well as provide gain control. Additionally, an active pFET load in series with a resistor is used to provide gain control.

The second stage is a source-follower buffer which is used in conjunction with a feedback resistor R_f to provide feedback to the input stage. The use of feedback makes it possible to provide a 50 Ω match at the input without the use of a traditional inductor, thus saving valuable silicon die area. Additionally, feedback helps to increase the bandwidth. However, there is a tradeoff between the selection of R_f for matching and noise [9]; the input impedance and the input referred current noise of the LNA are given by;

$$Z_i(\omega) = \frac{Z_f(\omega)}{1 + A_v(\omega)} \quad (1)$$

$$i_{n_{ref}}^2 = i_n^2 + \frac{4kT}{R_f} + \frac{v_n^2}{R_f^2} \quad (2)$$

The input impedance $Z_i(\omega)$ is proportional the feedback

impedance and inversely proportional to the open loop gain of the input stage. From equation (1), it can be seen that the feedback resistor and the gain can be chosen such that the input impedance is low and close to the desired 50 Ω . However, from equation (2), the input-referred current noise is minimized when R_f is large. To achieve the desired match and reasonable NF, a feedback resistance of 170 Ω was chosen.

The third stage consists of another CE amplification stage with shunt peaking provided by an inductor at the collector node as well as emitter degeneration to further increase bandwidth.

Further details on gain control and input match tuning mechanisms are shown in Fig. 2. Specifically, gain control is achieved by controlling the gate voltage (V_{Gate}) of the pFET device and thereby to control channel inversion. This has the effect of decreasing the impedance seen at the collector node of the CE transistor, which allows RF energy to travel through the pFET and into the VCC decoupling caps highlighted in Fig. 2. Input match (S_{11}) tuning is achieved using capacitive degeneration. As seen in Fig. 2, the capacitive load is generated by a capacitor in series with a varactor. Applying a bias voltage to the varactor changes the impedance and shifts S_{11} . This mechanism can be used to fine tune the input matching for matching-sensitive applications.

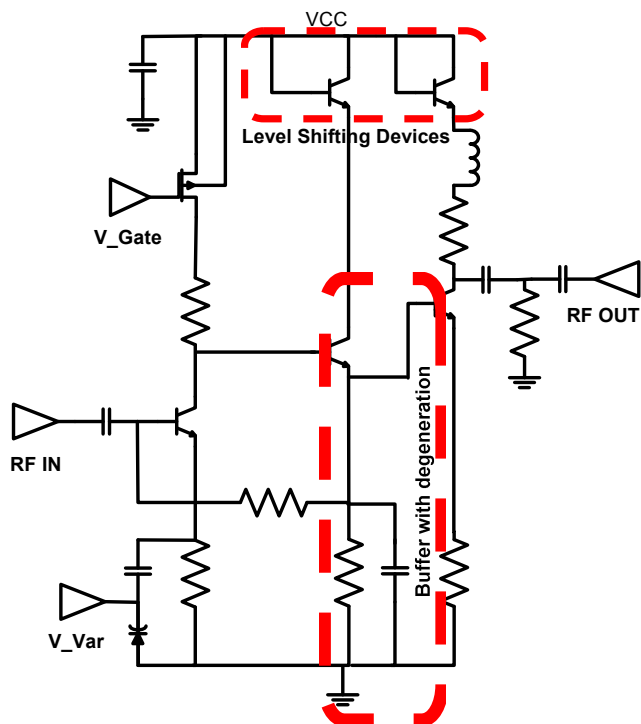


Fig. 1. Schematic of the SiGe LNA presented in this work.

III. MEASUREMENT RESULTS

The SiGe UWB LNA was implemented in a six-layer metal, 0.18 μm , 150 GHz SiGe BiCMOS platform. The chip area is approximately 1.06x0.09 mm^2 including pads. A photomicrograph of the circuit is shown in Fig. 3. The LNA

was tested using a HP 8510C Network Analyzer, along with 50 GHz cables and probes. The SiGe LNA operates from a 3.3 V supply. The measured current drawn by the LNA was 35.2 mA, resulting in a total power consumption of 116 mW.

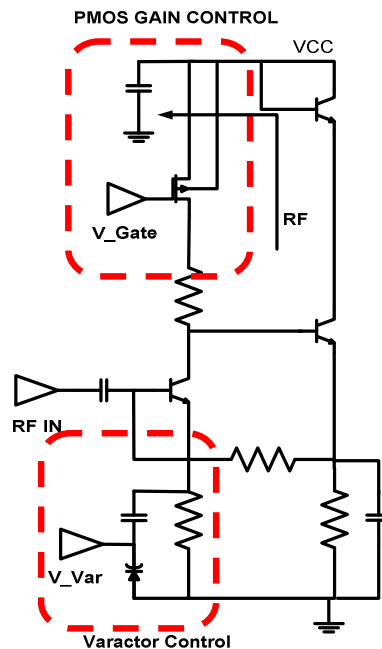


Fig. 2. Schematic of SiGe LNA input stage.

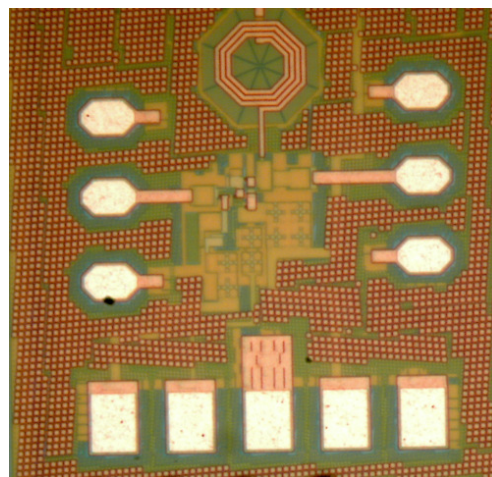


Fig. 3. Die micrograph of UWB SiGe LNA.

The S-parameters of the LNA were measured using an Agilent PSA along with 50 GHz cables and probes. Shown in Fig. 4 are the measured S-parameters of the UWB LNA with the control voltages V_{Gate} and V_{var} both set to 0 V. The gain of the LNA is 16.2 dB at 3 GHz and 16 dB at 20 GHz. The LNA demonstrates a maximum gain of 21.3 dB at 5 GHz and a mid-band gain of 19.1 dB at 11 GHz. The 3 dB bandwidth is 12.4 GHz from 3.4-15.8 GHz.

The LNA is well-matched over the frequency range of

interest. The input return loss, S_{11} , is less than -10 dB from 5 to 20 GHz. The input return loss is best matched at 13.4 GHz. The output return loss, S_{22} , is less than -10 dB from 5.0-14.0 GHz and is -8 dB at 20 GHz. S_{22} is best matched at 5.9 GHz. S_{11} and S_{22} are both less than -4 dB from 3-5 GHz. The gain flatness can be further improved with an improved input match, and will be explored in a future revision of the circuit.

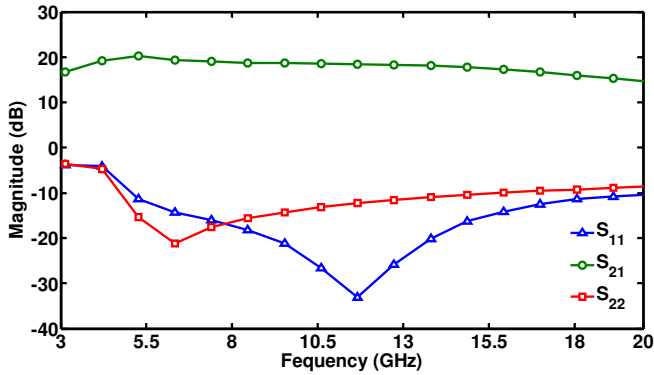


Fig. 4. Measured S-Parameters of the SiGe LNA.

The gain control feature of the LNA is illustrated in Fig. 5, which shows the stepwise decrease in the gain of the LNA with V_{Gate} voltage from 0.5-2.5 V. The LNA achieves a very wide gain control tuning range.

The gain of the LNA can also be adjusted by varying the V_{Var} voltage. Fig. 6 shows the decrease in gain with the increase in V_{Var} from 0.5-2.5 V. The gain variation from V_{Var} is smaller than that for V_{Gate} , V_{Var} can be used to make finer adjustments in gain, as needed.

However, use of V_{Var} has a greater impact on the input return loss. Fig. 7 plots S_{11} with V_{Var} voltage ranging from 0-2.5 V. The input match can be moved approximately 3 GHz from 13 – 10 GHz with V_{var} set from 0-2.5 V. This demonstrates that the present LNA can be used to adjust the input match to mitigate potential changes due to process variation or for dynamic adjustments that may be required based on the specific application or operating environment.

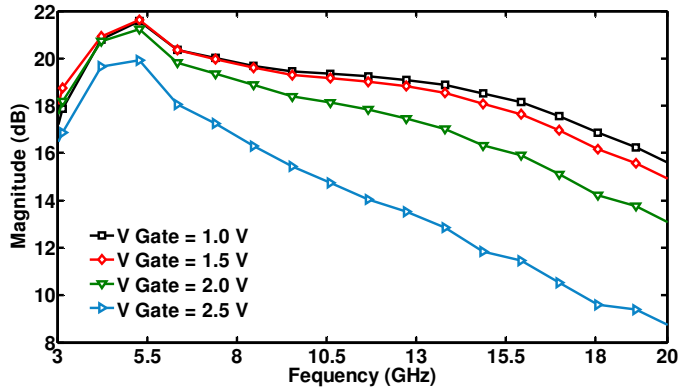


Fig. 5. Measured Gain with V_{Gate} Voltage Variation.

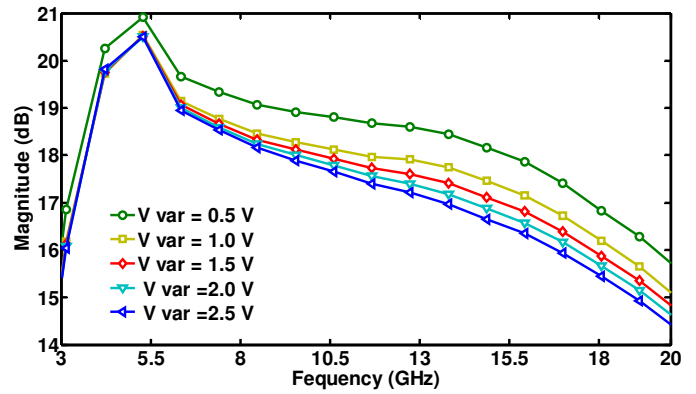


Fig. 6. Measured gain with V_{Var} voltage varying.

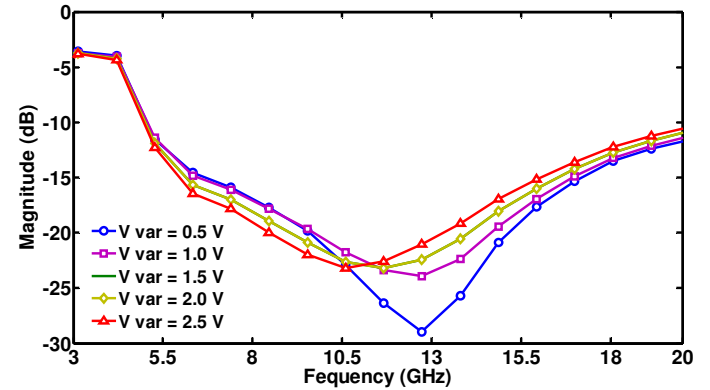


Fig. 7. Plot of S_{11} with V_{Var} varying.

The NF and Minimum Noise Figure (NF_{min}) are plotted in Fig. 8 for a frequency range of 8-18 GHz. This frequency range was chosen because it falls within the capabilities of our noise measurement equipment. The measured NF ranges from a minimum of 4.24 dB at 13 GHz to 5.19 dB GHz at 8 GHz and 18 GHz. Also plotted is NF_{min} , which ranges from 4.07 to 4.64 GHz, indicating that the LNA is reasonably well noise-matched over the 8-18 GHz frequency band.

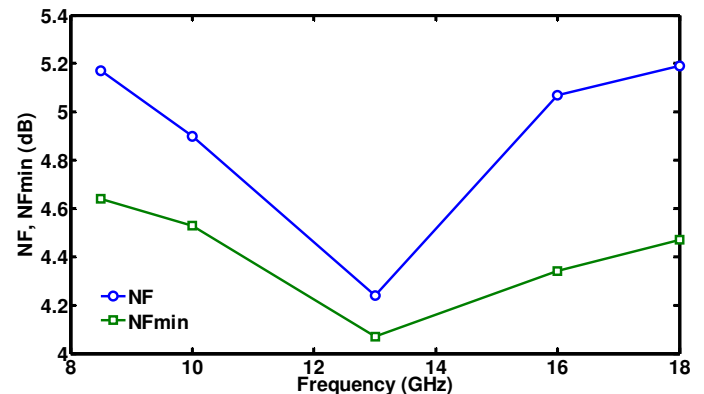


Fig. 8. Measured noise figure of the SiGe LNA.

The linearity (OIP3) of the LNA was also measured. Pout vs. Pin is shown in Fig. 9, with an OIP3 of 9.15 dB achieved for an input power of -6.47 dB.

A comparison of the present results with previous literature is shown in Table I. From the table it is shown that the NF and Gain of the presented LNA is very competitive with similar state of the art designs. In addition, for its bandwidth of 17 GHz, mid-band gain of 19.1 dB and NF of 4.2-5.2 dB, this SiGe LNA is very competitive in power consumption.

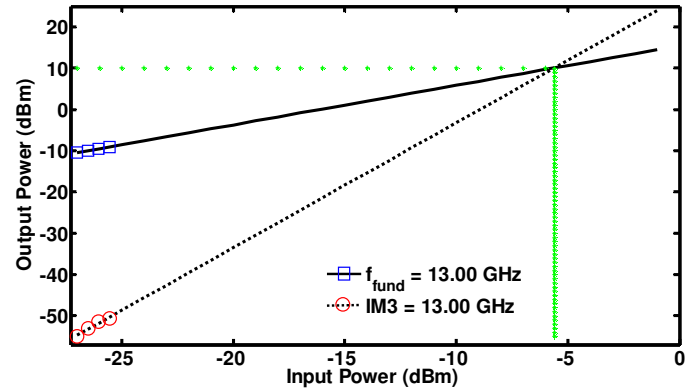


Fig. 9. Pout vs. Pin data for the SiGe LNA.

TABLE I
Comparison with Other LNAs Operating in a Similar Frequency Band.

Reference	Bandwidth [GHz]	Gain [dB]	NF [dB]	Current [mA]	Power [mW]	Topology	Technology
[3]	2.7-9.1	10	3.8-6.9	-	7.0	Distributed	0.18 μ m CMOS
[4]	3.1-10.6	16	3.8-4.0	5.3	9.5	Common Gate	0.18 μ m CMOS
[6]	1.3-12.3	9.1	4.4-4.6	2.5	4.5	Stagger Compensation	0.18 μ m CMOS
[11]	0.6-22	7.3	4.3-6.1	-	52	Distributed	0.18 μ m CMOS
[12]	8-18	18.8	5	24	120	Cascode	0.35 μ m SiGe
[13]	2-12	11	8-10	40	132	Distributed	0.25 μ m SiGe
[14]	0.05-23.5	17	6	27.8	100	Feedback	SiGe
This Work	3-20	19.1*	4.2-5.2**	35.2	116	Feedback, Peaking, Degeneration	0.18 μm SiGe

*Mid-band Gain at 11.5 GHz. **NF Measured from 8-18 GHz

IV. SUMMARY

A wideband, low power SiGe LNA has been designed and presented. The LNA demonstrates a bandwidth of 17 GHz and has a maximum gain of 21.2 dB and a 3 dB bandwidth from 5-17 GHz. The noise figure ranges from 4.2-5.2 dB across the 8-18 GHz band. The LNA consumes 116 mW from a 3.3 V supply. The LNA utilizes novel techniques for gain control and incorporates a means for adjusting the input match that can be used to mitigate for the effects of process variation. This LNA can be used in both X- and C-band applications. The LNA was designed in a commercially-available 0.18 μ m SiGe BiCMOS process.

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