

A W-band LNA in 0.18- μm SiGe BiCMOS

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Abstract—This paper presents the design and implementation of a W-band LNA. Fabricated in a 0.18- μm SiGe BiCMOS technology, the five-stage LNA achieves a peak power gain of 19 dB with a 3-dB bandwidth from 70-97 GHz and a minimum noise figure of 9 dB. The LNA exhibits more than 10-dB gain and input return loss <-12 dB across the entire W-band (75-110 GHz). The SiGe LNA is suitable for several W-band applications including 77/79-GHz automotive radars and passive imaging in the 80-110 GHz window.

I. INTRODUCTION

The low noise amplifier (LNA) is a ubiquitous building block, present in nearly any wireless receiver architecture. Its main purpose is to provide a low noise figure (NF) and high enough gain such that the NF of all subsequent receiver stages does not degrade the cascaded receiver NF (as inferred analytically from Friis equation). Traditionally, millimeter-wave (MMW) front-end circuits have been designed using III-V semiconductors. However, with aggressive technology scaling resulting in silicon transistors with f_T/f_{MAX} exceeding 200 GHz, coupled with the low cost (at high volume) and the high level of integration that silicon provides, silicon-based MMW integrated circuits (ICs) have become of great interest in recent years. There are still many challenges facing silicon MMW ICs, especially the low transistor gain and lossy passive components due to the low-resistivity substrate. While 60-GHz silicon circuits have been heavily researched in the past few years due to their commercial potential [1], the focus is now turning to higher frequencies [2]-[4]. This paper presents the design and measurement of a SiGe LNA operating in the 75-110-GHz (W-band) frequency range. This LNA has several potential applications including 77-GHz long range radar, 77-81-GHz short-range radar, and W-band imaging in the 80-110-GHz atmospheric window.

II. LNA DESIGN

The design of an amplifier operating near half of the transistor cut-off frequency, while achieving sufficiently high gain and low NF, is extremely challenging. Figure 1 shows the maximum available gain (MAG) and minimum achievable noise figure (NF_{min}) of a common-emitter HBT in the technology used in this work. The device is optimally sized and biased such that it achieves the lowest NF_{min} for this technology. At 90 GHz, a MAG of 3.9-dB and an NF_{min} of

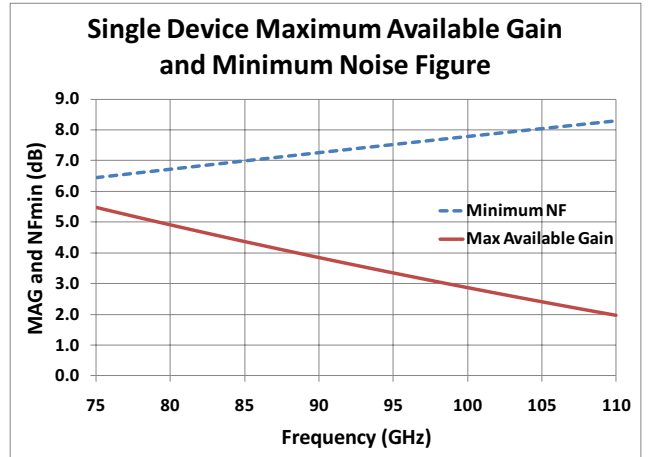


Figure 1. NF_{min} and MAG for an HBT in this technology.

7.2-dB are obtained. The aforementioned device performance has two major implications on LNA design. First, it indicates that a minimum of 4 stages are needed in order to realize an LNA with 15-dB gain (the goal of this work). Secondly, the first amplifier stage will not have sufficient gain to significantly reduce the NF contribution of the subsequent stage. The effect of the latter gain stages on the overall LNA NF can be estimated by using the transistor MAG and NF_{min} values in the well-known Friis equation for the cascaded NF of a multi-stage amplifier,

$$F = F_1 + \sum_{k=2}^N \frac{F_k - 1}{\prod_{j=1}^{k-1} G_j}, \quad (1)$$

where F_k and G_k are the noise factor and the power gain, respectively, of the k th stage. Using (1), it is calculated that the second stage will add at least 1.2 dB to the overall LNA NF. A third stage will contribute an additional 0.4 dB, and a fourth stage will add another 0.1 dB, resulting in theoretical 4-stage MAG and NF_{min} of 15.6 dB and 9.0 dB, respectively. The previous analysis assumes that each stage achieves maximum gain and minimum noise figure. However, by design, the first stage of an LNA will trade off a certain amount of available gain in order to achieve better noise match at the input. This, along with loss in the matching

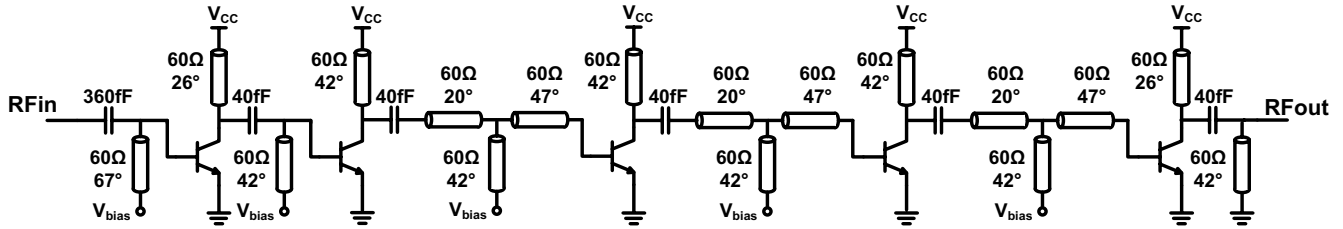


Figure 2. Schematic of the 5-stage LNA

networks, necessitates the use of a fifth gain stage in order to achieve the desired 15-dB gain. This additional stage has a negligible (<0.1 dB) contribution to the LNA NF.

The 5-stage LNA schematic is shown in Fig. 2. The input matching networks of the first two stages are designed to achieve minimum NF. Additionally, it is desirable to keep the topologies of these matching networks as simple and compact as possible in order to minimize any pre-gain losses (which will directly degrade the NF). To achieve the above goals, we use a different design methodology as compared to standard silicon-based techniques for obtaining simultaneous power and noise match [5]. Specifically, due to the low gain of the HBTs in the frequency range of interest, inductive emitter degeneration is not employed, thereby avoiding the associated reduction in gain. Instead, we first find the current density which minimizes the HBT NF_{min} . Next, the location of the optimum source reflection coefficient (Γ_{opt}) is plotted on the Smith chart, along with the device unmatched input reflection coefficient (Γ_{in}). The device size is then determined graphically using the Smith chart such that Γ_{opt} is within a predetermined constant-VSWR circle, and simultaneously Γ_{in} is on the same resistance (or conductance) contour. This choice of the device size will only require a single stub at the input in order to move the device Γ_{in} towards Γ_{opt} , thereby achieving excellent noise match. Since Γ_{opt} is within a predetermined acceptable VSWR circle, the matching network will simultaneously provide a good impedance match.

Following the methodology described above, an optimum HBT emitter area of $0.75 \mu m^2$ is found. As shown in Fig. 3,

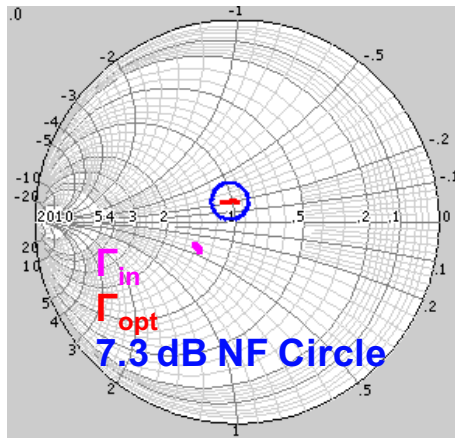


Figure 3. Unmatched reflection coefficient and optimum source impedance.

Γ_{opt} is located on the circle with a constant VSWR of 1.4:1, which corresponds to 15-dB input return loss. A short-circuited stub at the input moves Γ_{in} along a constant conductance contour such that it achieves an input noise match within 0.1 dB of NF_{min} , and an input return loss of 15 dB at 90 GHz.

An additional consideration at the input is the capacitance associated with the input bond-pads. In the W-band, this capacitance cannot be ignored as it will seriously degrade the input match. One method of addressing this issue is to include the pad capacitance as part of the input matching network design. Another method, which has been used in this work, is to use a t-line shunt stub in order to resonate out the bond pad capacitance at the operating frequency [6]. If designed properly, this method results in the bond-pads being matched to 50Ω , making them electrically transparent in a $50\text{-}\Omega$ system.

Starting with the output of the second stage, all subsequent inter-stage matching networks have a more complex topology. This topology is essentially a T-matching network implemented with transmission lines. It has more degrees of

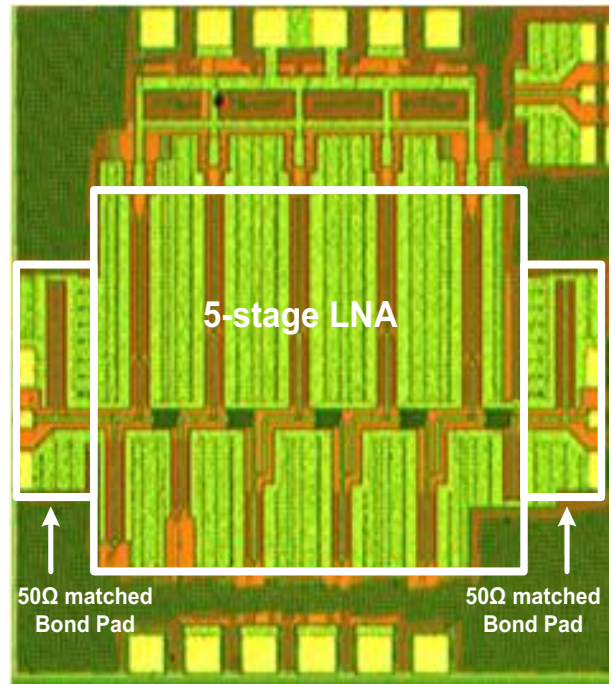


Figure 4. Die micrograph of the LNA.

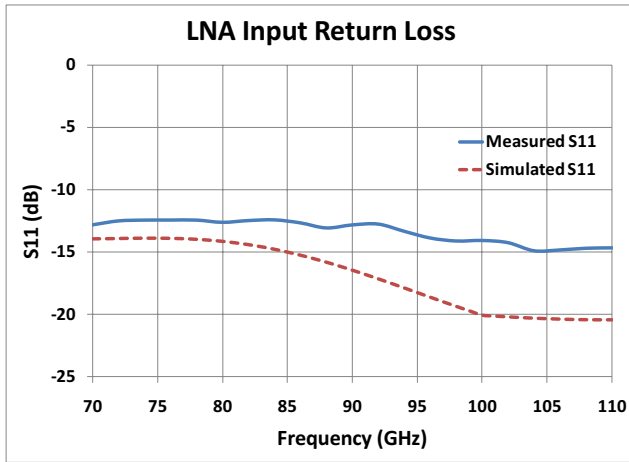


Figure 5. Measured and simulated input return loss.

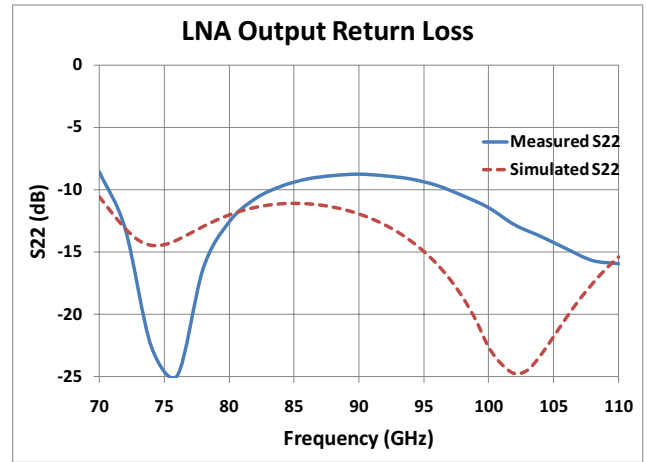


Figure 7. Measured and simulated output return loss.

freedom than a single-stub matching network, and therefore enables conjugate matching between the output of each stage and the input of the subsequent stage over a larger bandwidth than a single-stub matching network. This enables maximum power transfer, and hence maximum gain, from the last three stages. The insertion loss of the series transmission lines in the T-match should be minimized, since this loss will reduce the amplifier gain. To this end, transmission lines were implemented as slow-wave coplanar waveguide (CPW) structures [7]. EM simulations show that at 90 GHz, a slow-wave CPW t-line achieves 40% higher phase-shift than standard conductor-backed CPW t-lines, for a given length. This translates to physical line lengths (in the matching networks) being reduced by 40%, which reduces both loss and chip area.

The SiGe technology used in this work provides metal-insulator-metal (MIM) capacitors with a density of $2.0 \text{ fF}/\mu\text{m}^2$. The MIM capacitors are used to implement the 360-fF decoupling capacitors. The 40-fF capacitors are implemented as lateral inter-digitated capacitors. These capacitors separate the DC bias voltages of adjacent stages and are absorbed into the inter-stage matching networks.

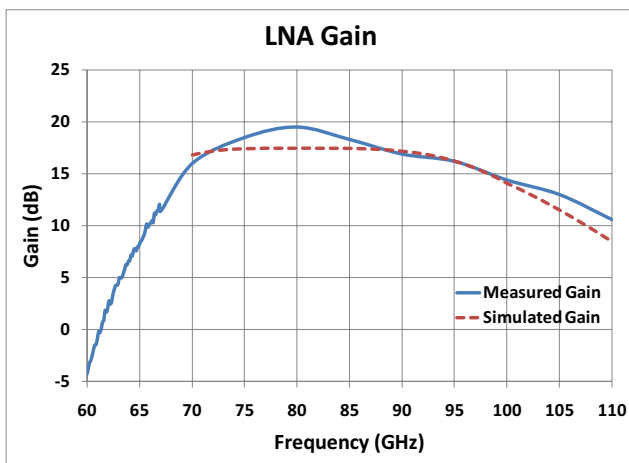


Figure 6. Measured and simulated gain of the LNA.

III. MEASUREMENT RESULTS

The LNA has been fabricated in a $0.18\text{-}\mu\text{m}$ SiGe BiCMOS process with six metal layers. The die micrograph of the LNA is shown in Fig. 4.

On-wafer LNA measurements were performed using three different test setups. The first setup uses a VNA with W-band frequency extenders to measure S-parameters from 70-110 GHz. The VNA measurement results (Figs. 5-7) show a peak gain of 19 dB at 80 GHz, and better than 12 dB input return loss and 9 dB output return loss from 70 to 110 GHz. The measured S-parameters are in good agreement with the simulations.

In the second setup, a 12-18-GHz signal generator drives a times-6 multiplier, which provides a W-band input signal to the LNA. A spectrum analyzer at the LNA output is used to measure the output power. This setup is used as an alternate method for measuring LNA gain, and also for compression measurements (Fig. 8). The compression measurements were performed at 80 GHz, and show a peak gain of 20 dB with an input-referred 1-dB compression point of -35 dBm .

The third test setup uses a spectrum analyzer (Agilent

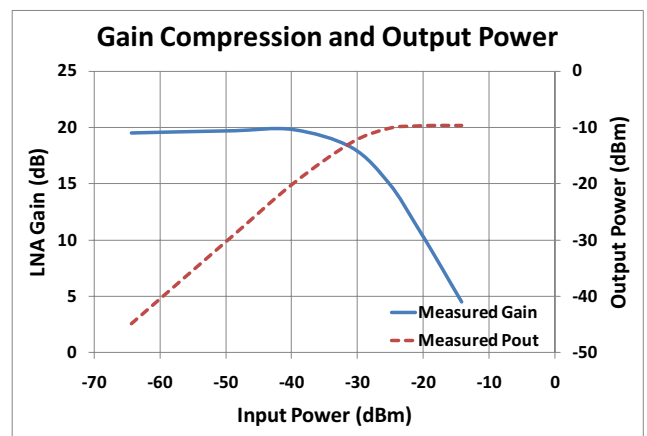


Figure 8. Measured gain compression and output power.

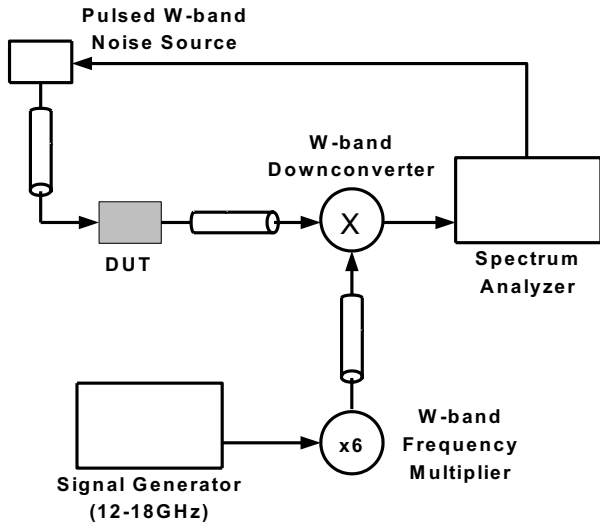


Figure 9. Test setup for noise figure measurement.

E4448A) with noise figure measurement personality and an external down-converter in order to perform W-band noise measurements, as shown in Fig. 9. Measurements show a minimum NF of 9 dB at 90 GHz, which corresponds to the theoretical minimum achievable 5-stage NF calculated earlier. Note that the measured NF data is only shown for frequencies up to 95 GHz. This is because the noise figure of the external down-converter is extremely high (30dB) at frequencies over 95 GHz. This high down-converter NF made calibration difficult and resulted in a high degree of measurement uncertainty.

IV. CONCLUSIONS

A W-band LNA has been demonstrated in a 0.18- μm SiGe BiCMOS technology. The LNA draws 35-mA of current from a 1.8-V supply with a chip area of 1.0 mm^2 (not including bond pads). Measurement results of the fabricated LNA prototype show good agreement with simulations. The LNA has a minimum measured NF of 9 dB, a peak gain of 19 dB, a 3-dB bandwidth of 70 to 97 GHz, and more than 10 dB of gain up to 110 GHz. The SiGe LNA can be used in 77-GHz long-range and 79-GHz short-range automotive radars, as well as in passive imaging receivers operating in the 80-110-GHz window.

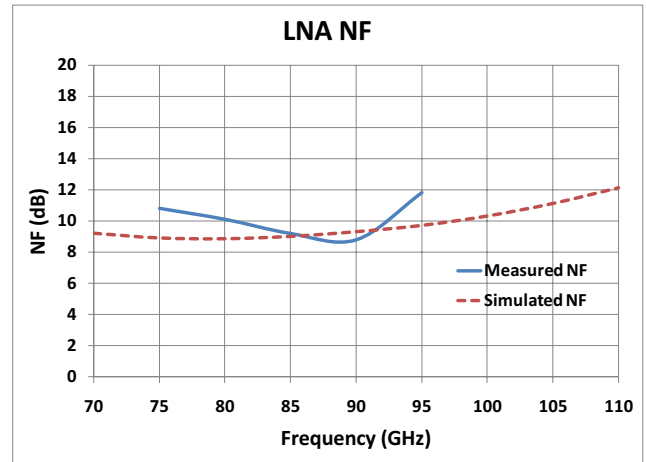


Figure 10. Measured and simulated noise figure of the LNA.

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