SEMICONDUCTOR

Accurate LDMOS Modeling in BCD Technologies

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Outline

- Motivation
- Jazz LDMOS Model Description
- Jazz Power Device Design Flow
- Power Switching and Gate Charge

Motivation

BCD Power Design Enablement

Physical, Scalable Compact LDMOS Models

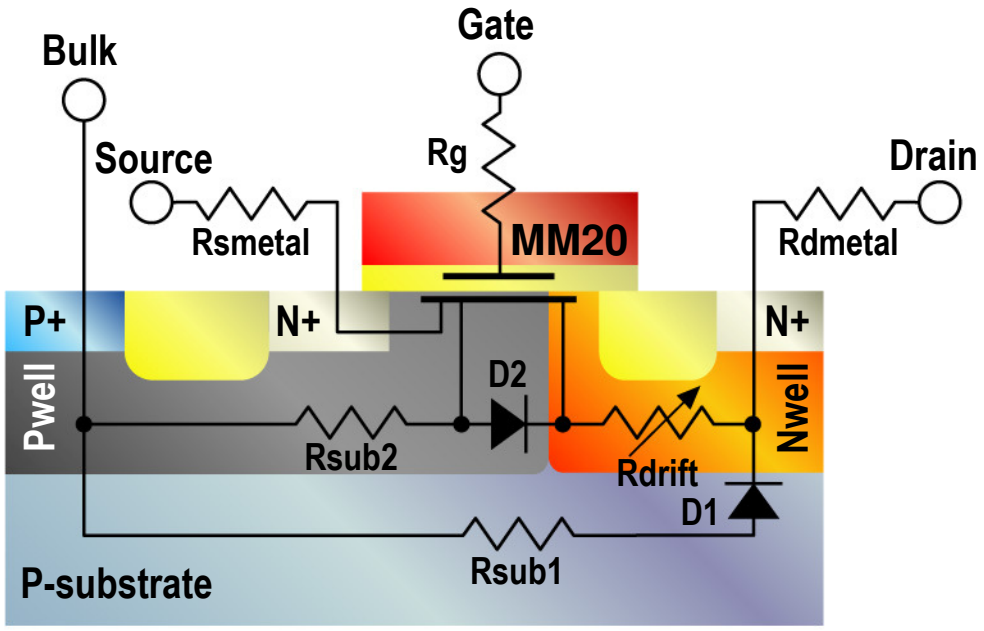
- Assymetric gate capacitance
- Scalable nonlinear drift region
- RDSon vs. breakdown voltage
- Process variation

Enabling Power Cell Design Flow

- Scalable PCELLs to optimize RDSon vs. BV
- CDF design aids for RDSon sizing and BV calculation
- Accurate simulation of power cell layout

Jazz HV/RF LDMOS Model

- NXP MM20 includes intrinsic channel and gate poly overlap of thin oxide drain region
- Physically models unique ldmos D/S charge partitioning
- Includes Self-heating



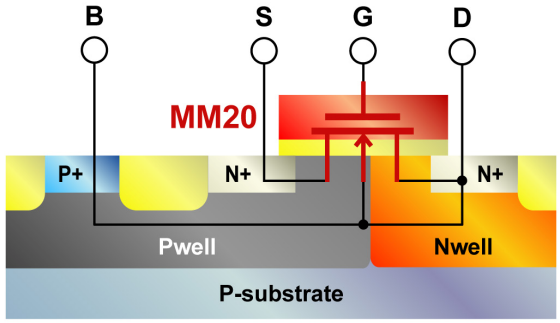
- Jazz developed physical, scalable model for extended drift region which includes nonlinear quasi-saturation effects
- Scalable metal resistance models
- Substrate and gate network provides accurate RF modeling

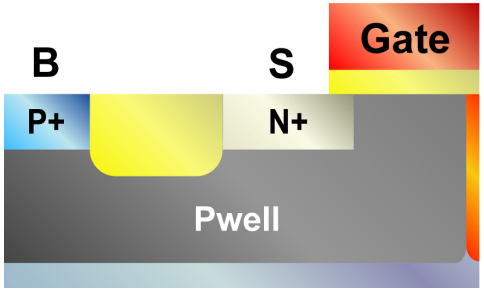
MM20 Model Features

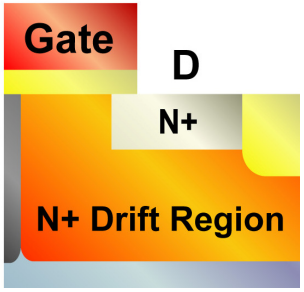
MM20

- Surface potential based
- Physical charge sharing between channel and drift region
- 1/f, thermal, gate-induced noise
- Geometry and temperature scaling
- Self-heating and breakdown models

Jazz is the First Foundry to Announce Support!







Channel

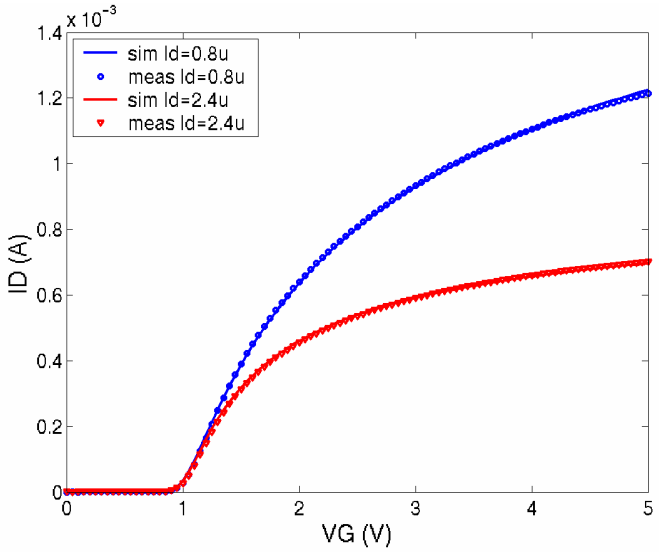
- Vertical field mobility reduction
- Velocity saturation, CLM and DIBL
- Avalanche model

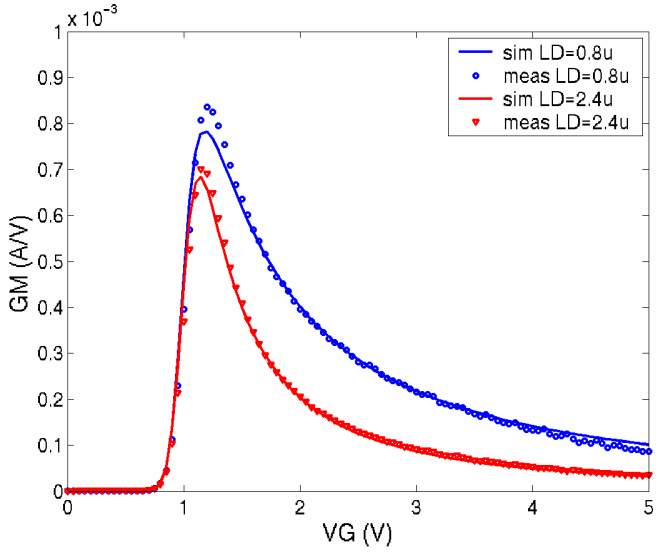
Gate Controlled Drift Region

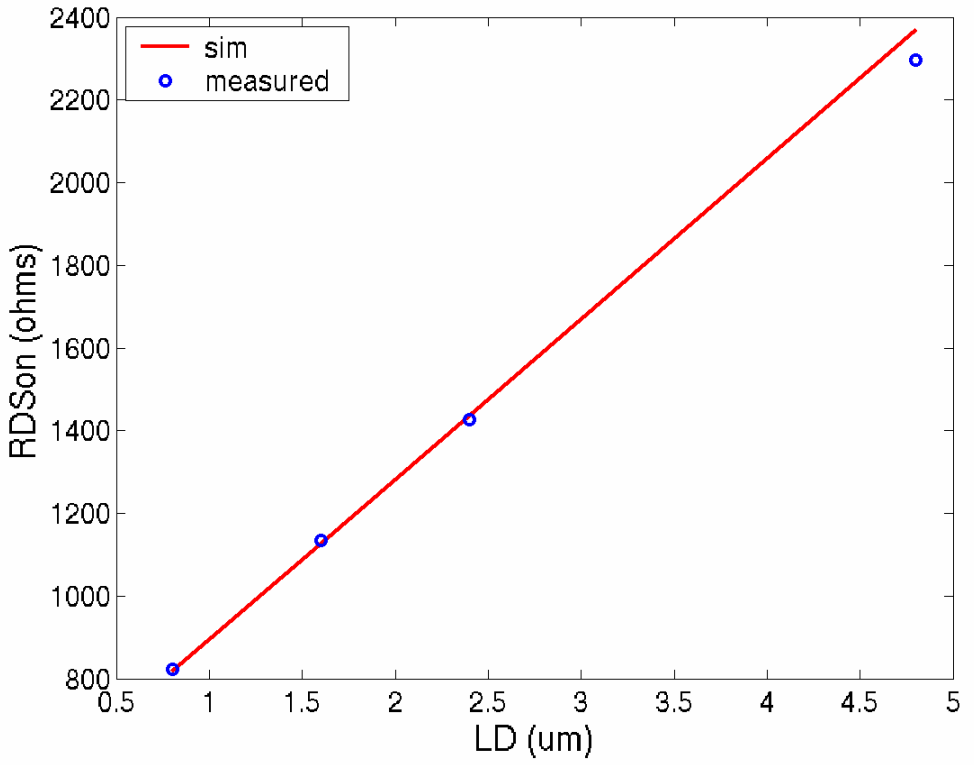
- Accumulation/depletion
- Bulk current
- Vertical field mobility reduction
- Velocity (quasi) saturation
- Avalanche model

Source: NXP, TU/e

Scalable Ldrift Region Model Results







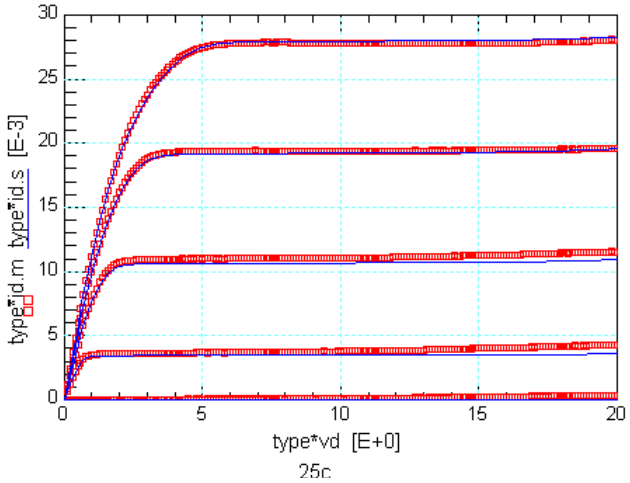
Accurate Prediction RDSon vs. LD

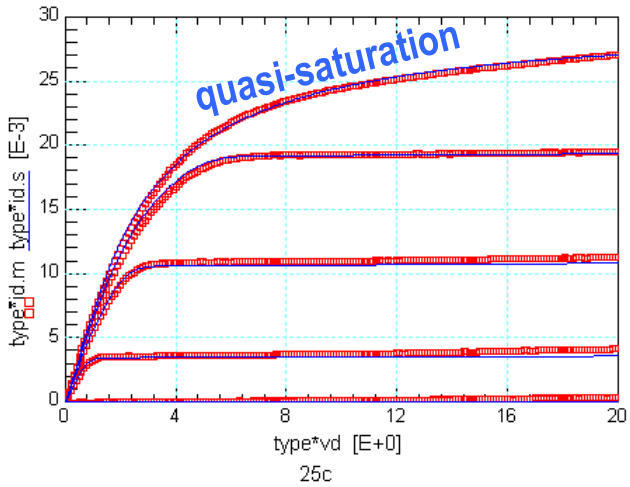
Scalable Ldrift Region Model Results

Ldrift=0.8µ

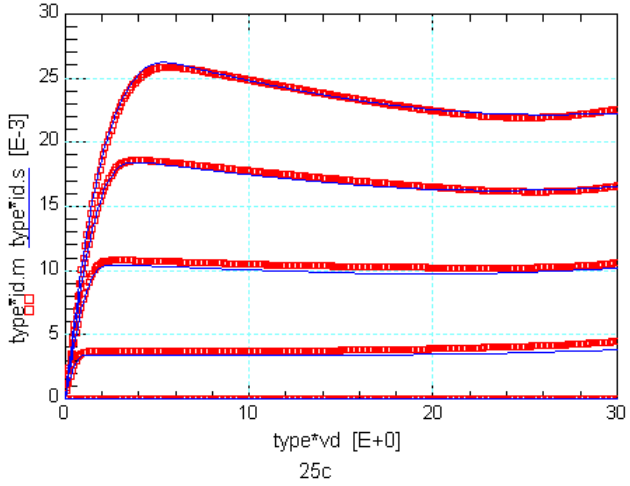
Ldrift=2.4µ

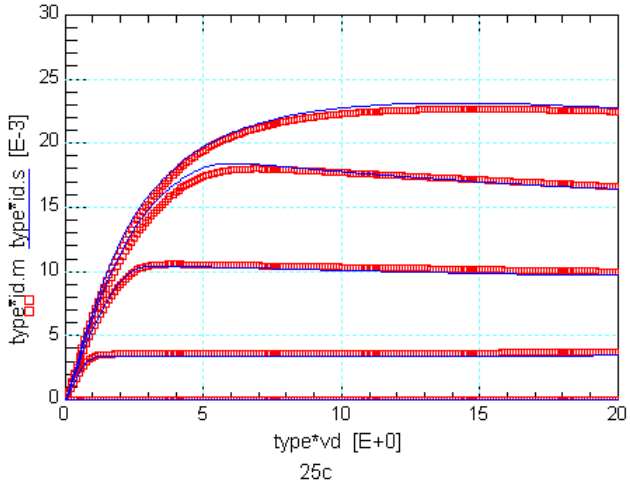
Pulsed



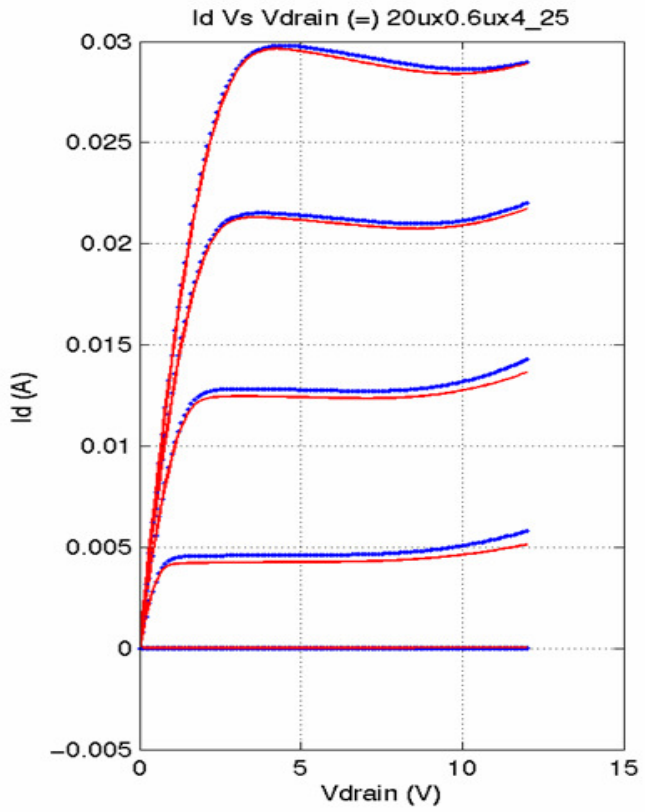


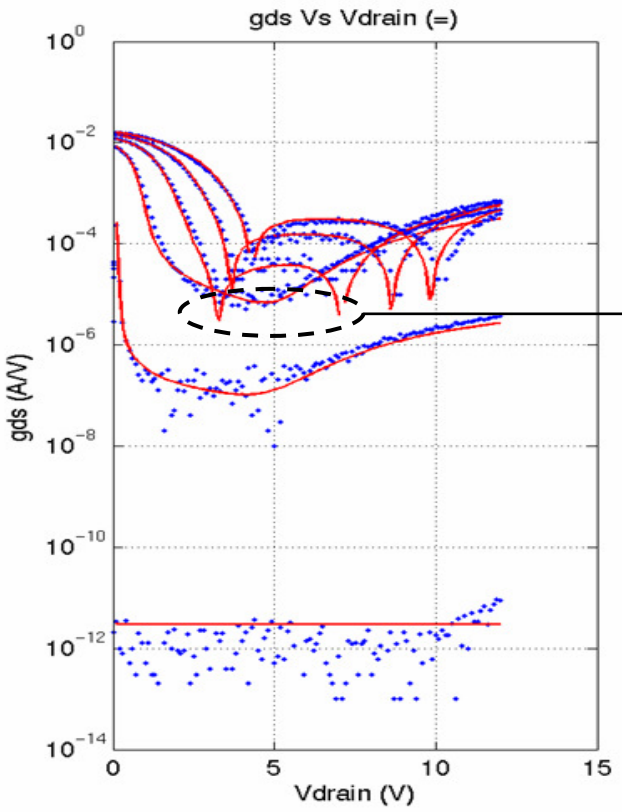
Non Pulsed





Self-Heating, Breakdown





Dual conduction sign change from Self-heating and Breakdown

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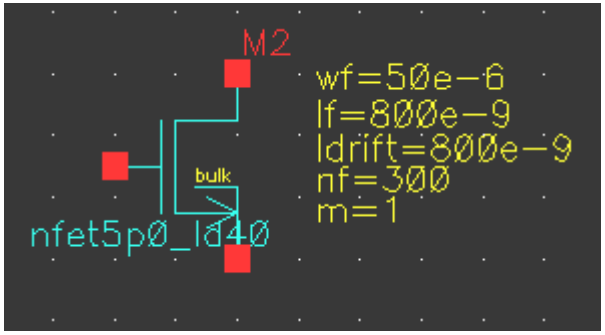
BCD HV LDMOS RDSon Design Flow

BCD 20-40V HV LDMOS
Design Kit Implementation Design Flow: Schematic



CDF Parameter	Value
Model Name	n540hv_s
Multiplier	1
Fingers	300
Finger Width	50u M
Length	800n M
Drift Length	800n M
Max Vds Estimate	20 V
Rds On Estimate	1.052317 Ohms
Thermal Resistance Option	0
Post Layout Parasitics?	0

Scalable Ldrift

- BV=F(LD) estimate calculation
- Direct BV vs. RDSon information

RDSon Calculator

- Provides CDF design tool for RDSon sizing as F(Wf, LD, Nf, M)
- Ideal RDSon vs. RDSon with metal
  - Direct Measure of Layout Quality

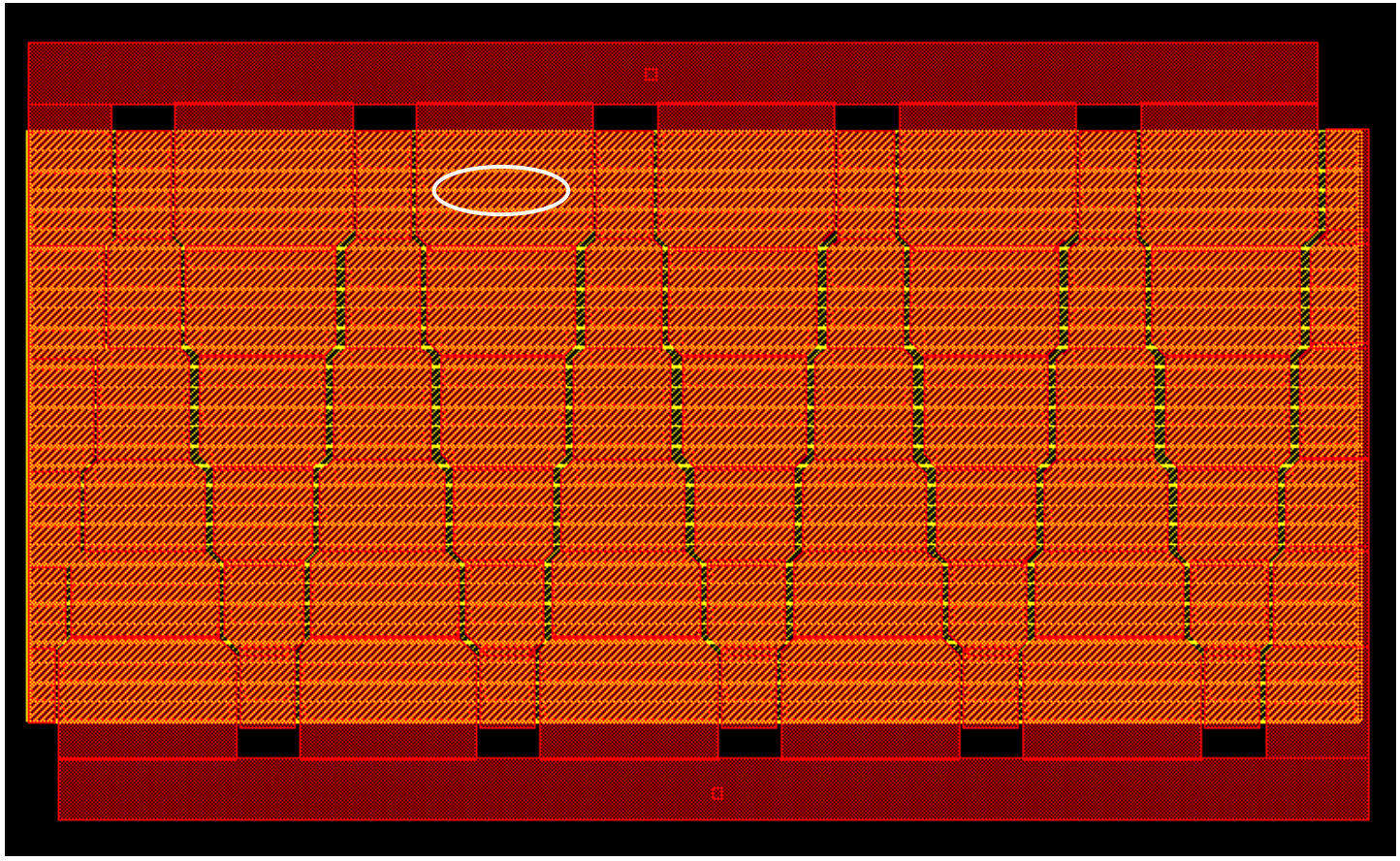
Design Flow: Layout

28 mΩ Power Transistor

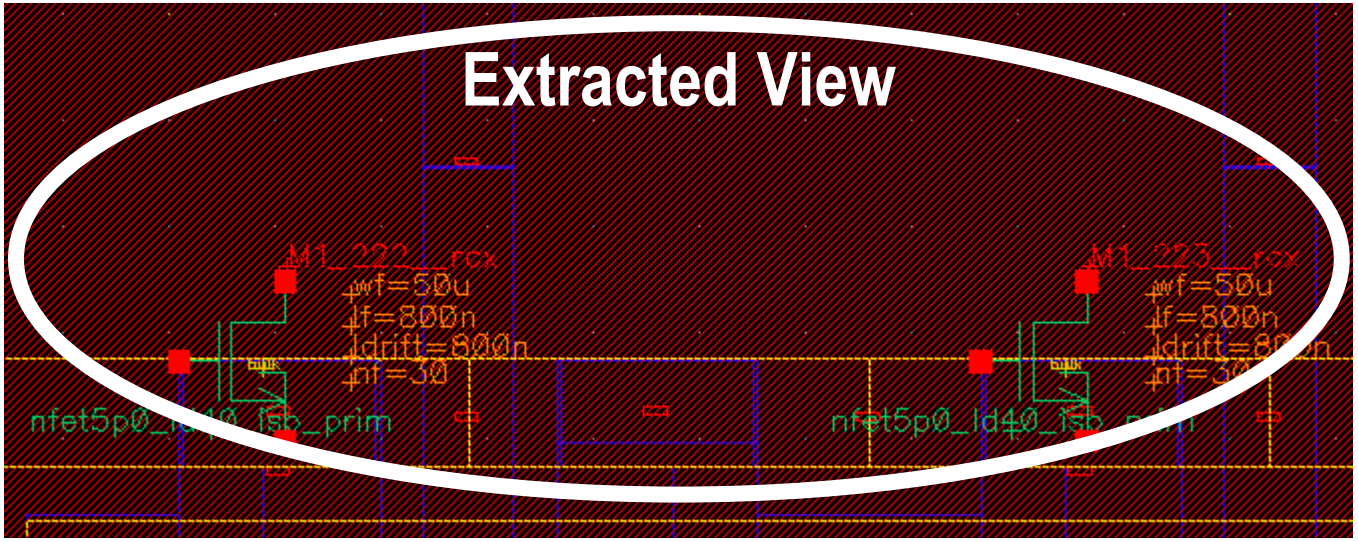
Metal 2 and Metal 3 Fingers Reduce RDSon

Metal tapering provides optimization of

- resistance
- capacitance
- current handling



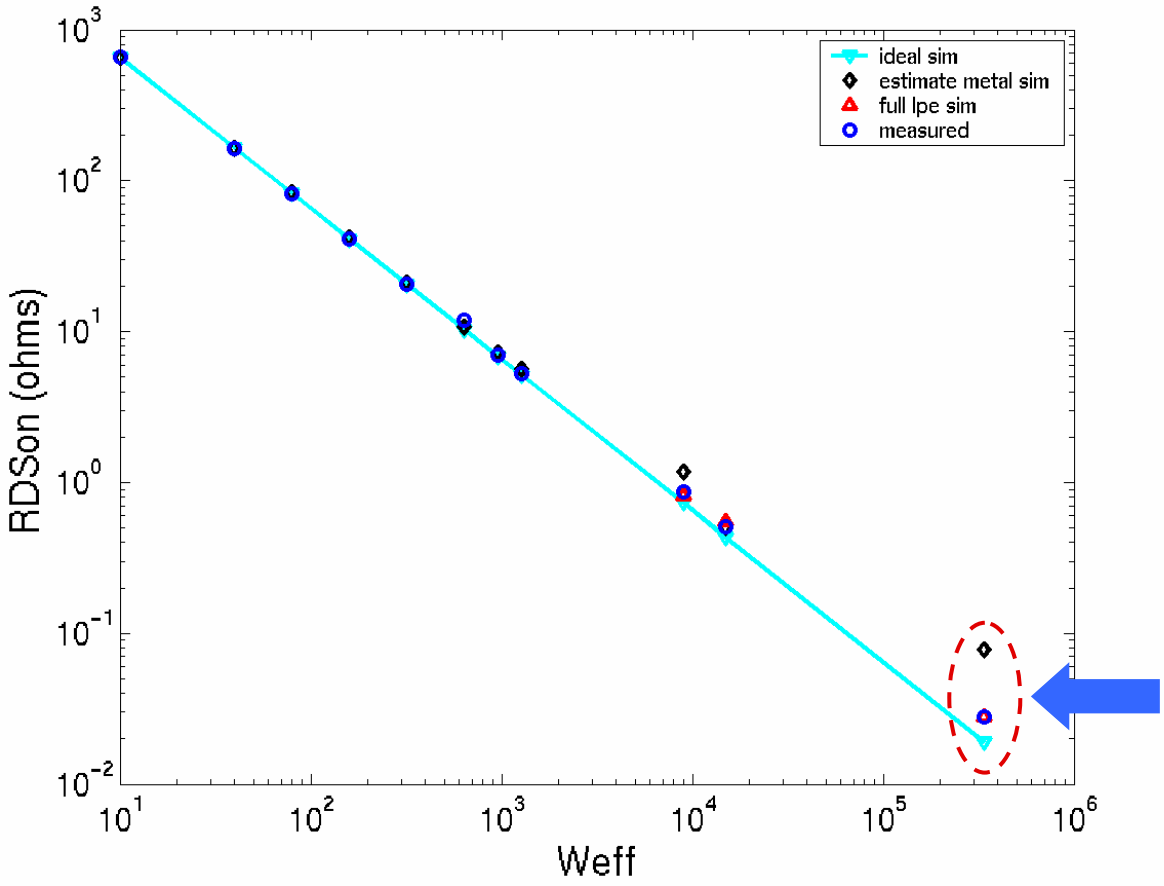
Design Flow:
Layout Post Extraction and Simulation



Postlayout=1 flag passed to model, turns off estimated metal Parasitics

Precise Layout Parasitics extracted in LPE by Assura RCX or Calibre PEX

RDSon Scaling Measurements – Simulations



Large Power Cells use M3-M2 routing

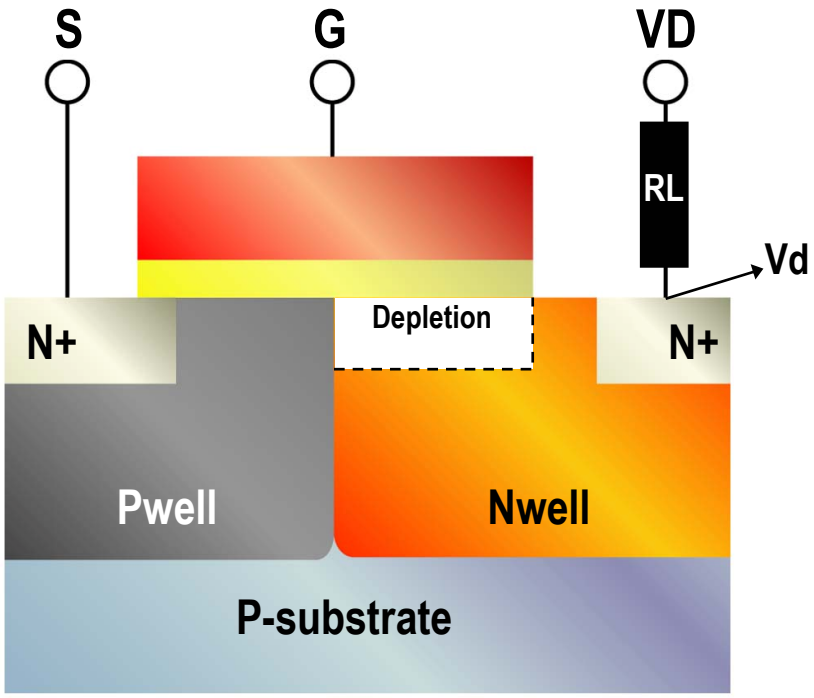
Estimated Pre Layout Simulation – M2 only

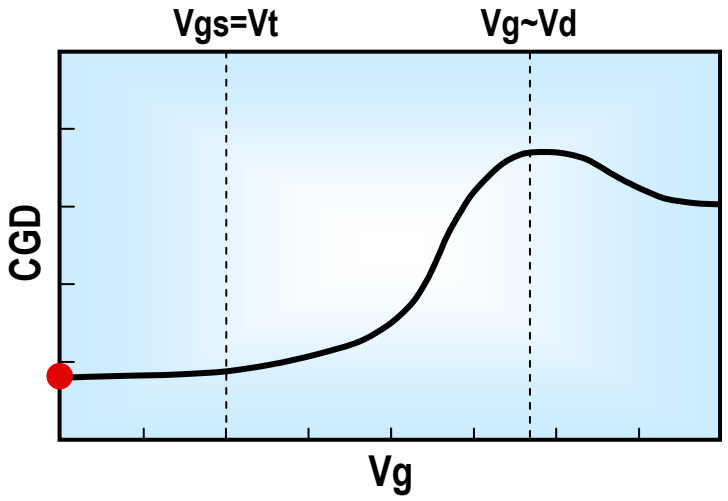
LPE Simulation Closes Gap for Large Cells

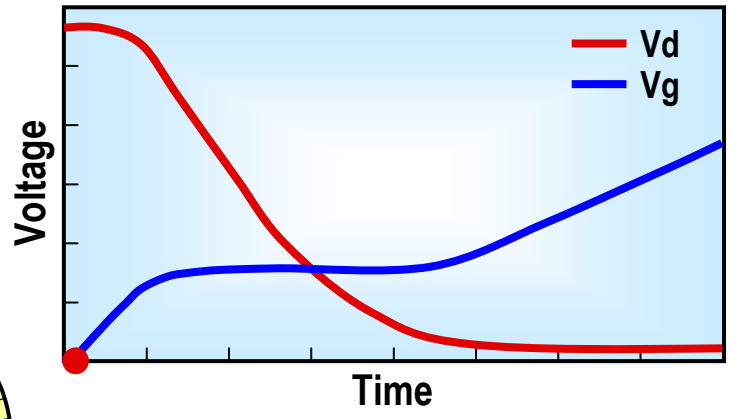
Weff = Wf x Nf x M
50µ x 300 x 15
~30% Rmetal

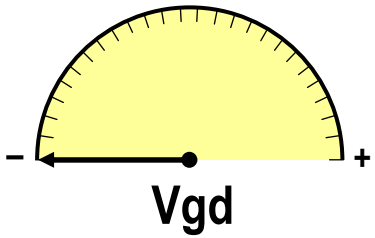
Understanding Power Switching and Gate Charging

LDMOS Switching – Gate Charging

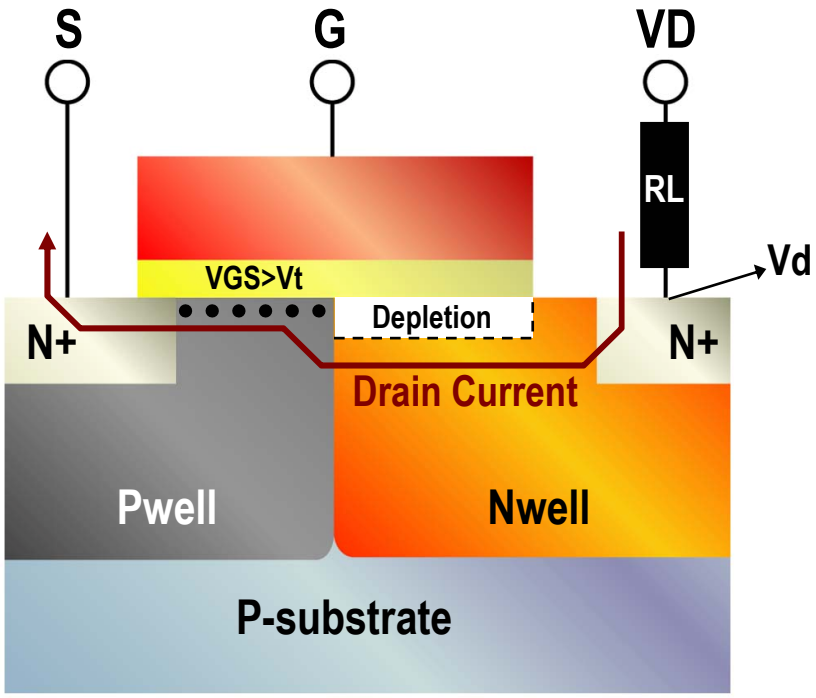


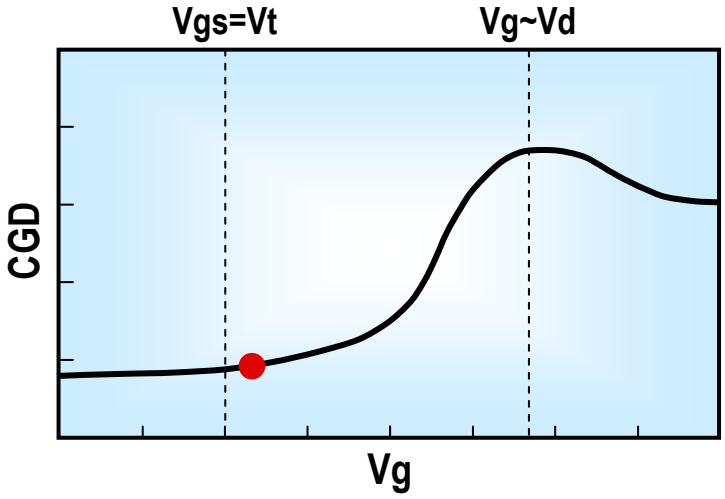


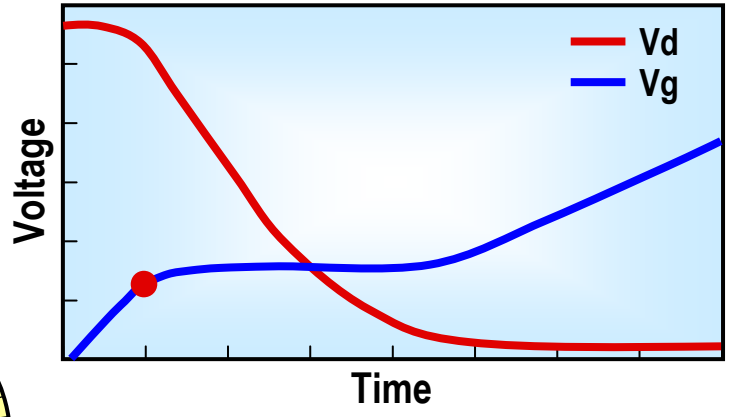


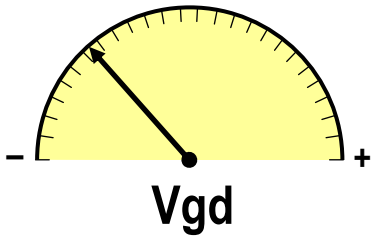


LDMOS Switching – Gate Charging









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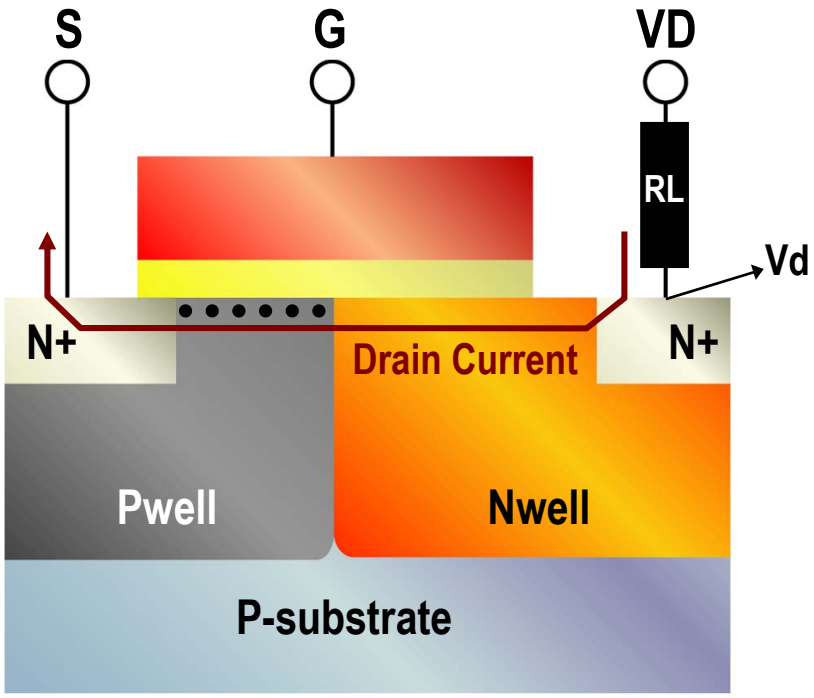

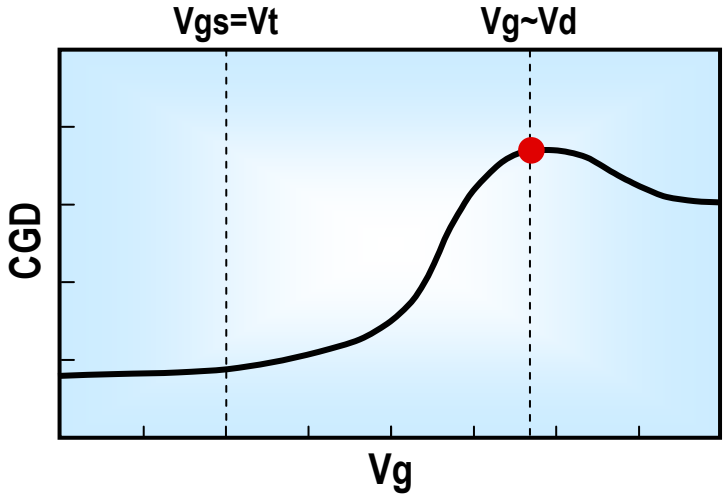

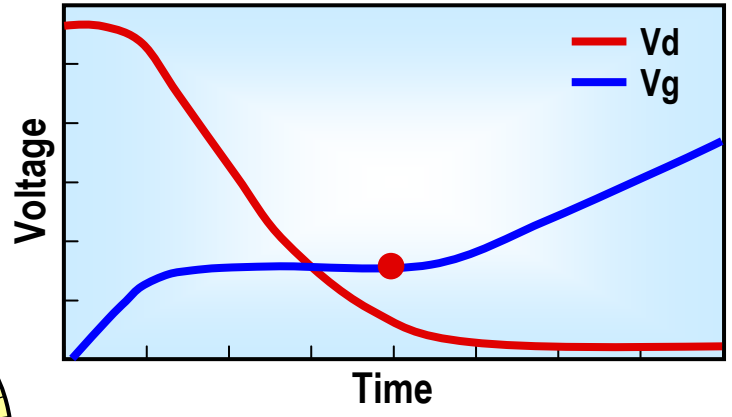

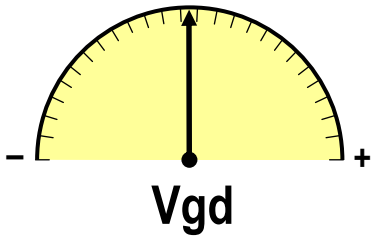

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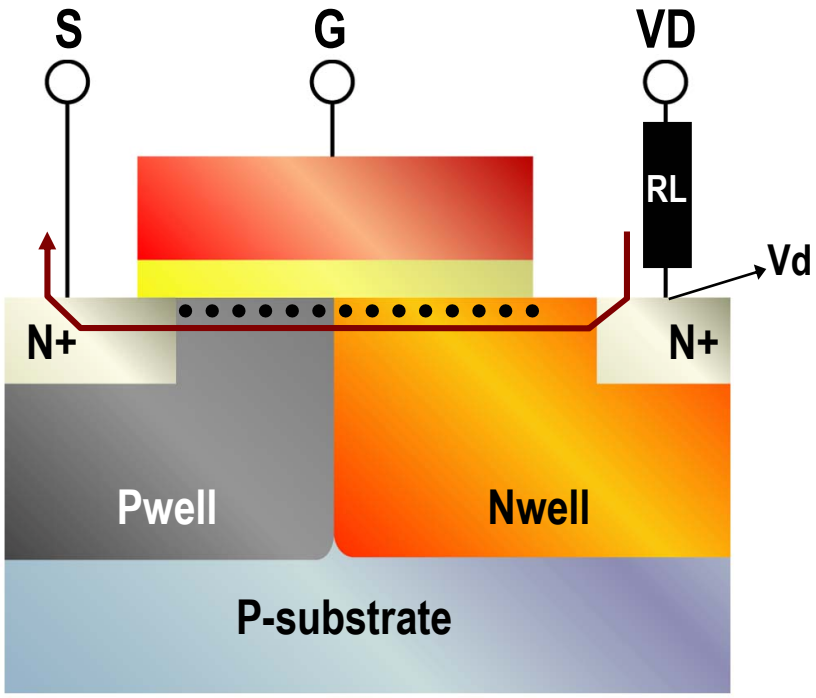
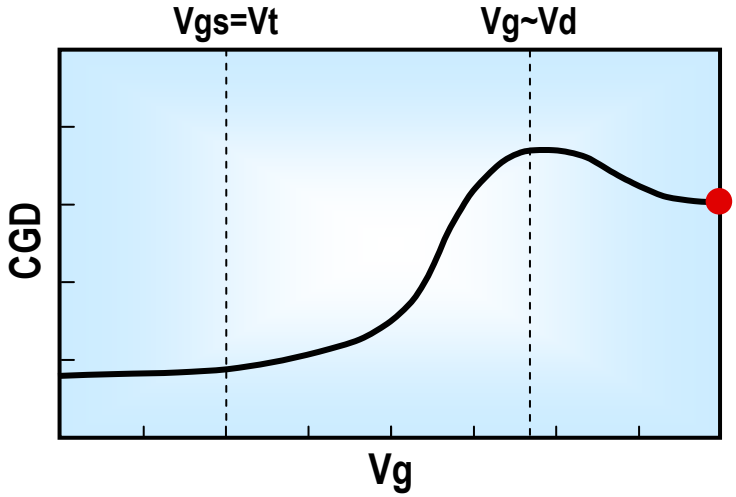
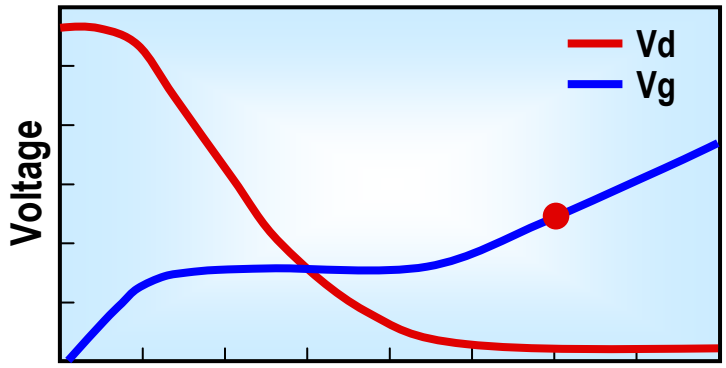
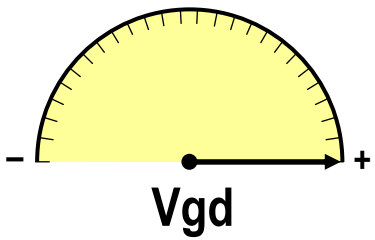
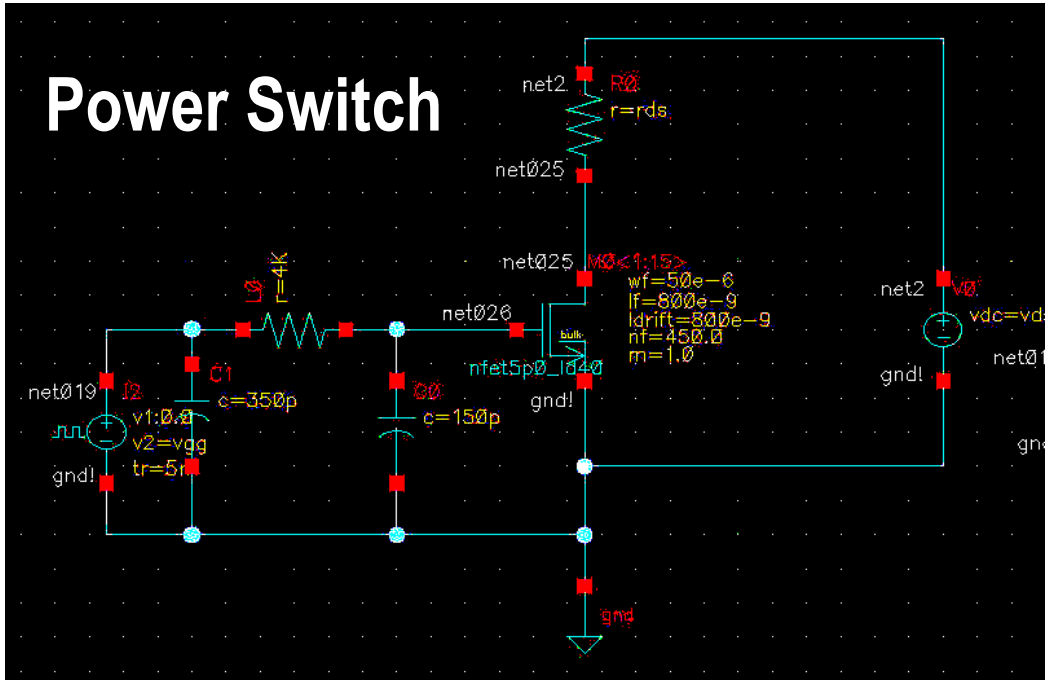


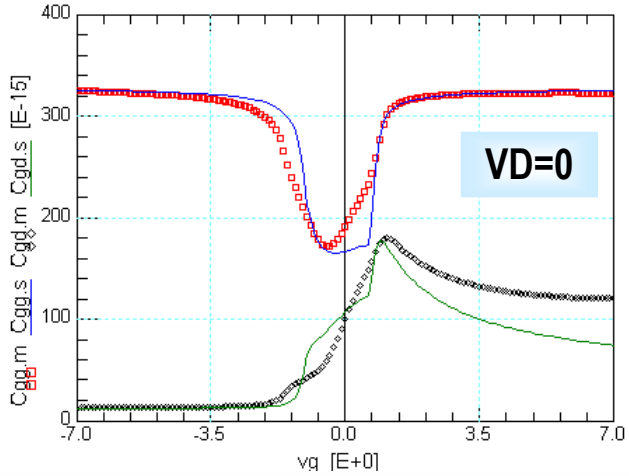


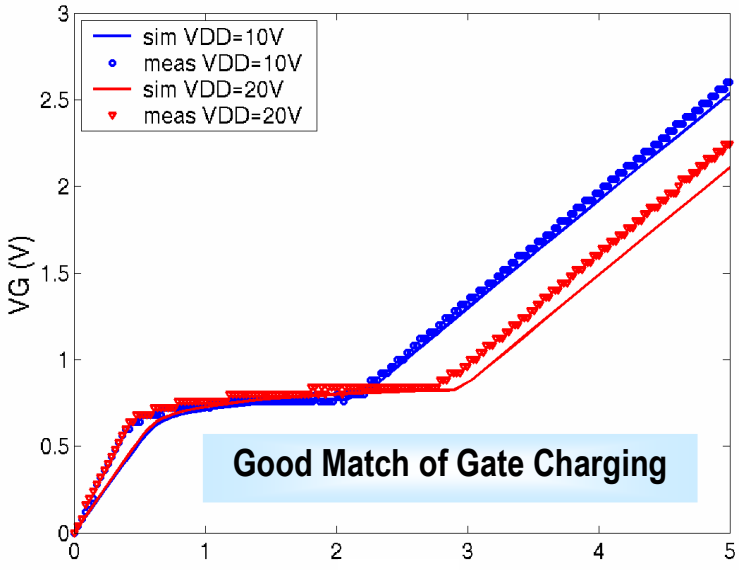




Gate Charging/Capacitance Measurements – Simulations







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