

# An 11.1Gbps Analog PRML Receiver for EDC of up to 400km-Reach WDM Fiber-Optic Links

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**Abstract**—A dispersion tolerant receiver for fiber-optic links, in 0.18 $\mu\text{m}$  SiGe BiCMOS, implements a Class-2 Partial Response Maximum Likelihood (PRML) equalization entirely in the analog domain. Post-FEC error free operation is achieved with data received from over 400km of uncompensated single mode fiber (SMF). The receiver complies with XFI Jitter specifications for Telecom (SONET OC-192 and G.709 “OTU-2”).

## I. INTRODUCTION

Chromatic and polarization mode dispersion in optical fiber causes inter-symbol interference and subsequently leads to errors at the receiving end of the channel. Optical dispersion compensation requires inconvenient and expensive compensation modules commonly placed at 80km intervals. Electrical Dispersion Compensation (EDC) provides for a simple low cost solution by replacing expensive optics with inexpensive electronics. Recently, maximum likelihood sequence estimation (MLSE) techniques have evolved as the preferred approach for high-performance EDC in 10Gb/s fiber-optic systems [1-2]. Previously reported EDC receivers employ an analog front end including a VGA and an ADC followed by a DSP. The reported solutions are either based on a dual-chip solution or are entirely implemented on a single chip using an advanced CMOS process. They utilize a narrow sliding window for their digital implementation of the Viterbi Decoder resulting in suboptimal performance. In this paper, we present a single-chip small form factor (2.5mm x 2.5mm die) solution, in which the MLSE decoding function is implemented entirely in the analog domain on a mature 0.18 $\mu\text{m}$  SiGe process. Our approach augments the MLSE with partial-response equalization. This kind of multi-stage equalization results in a reduced-complexity, superior-performance solution compared with the MLSE-only approach. Some aspects and blocks of the IC were previously reported [3-6]. This presentation aims to show the entire receiver architecture as well as to describe blocks and functions not covered in previous publications.

## II. ARCHITECTURE

The simplified block diagram of the IC is shown in Fig. 1. The dispersion impaired optical data signal from the fiber is converted to the electrical domain by a transimpedance amplifier (TIA) and is fed to the 50 $\Omega$  terminated variable-gain amplifier (VGA) for amplitude normalization and then enters a Continuous Time Filter (CTF) to undergo normalization of the frequency response.

A 5-tap discrete time FIR filter provides for further equalization and is responsible for sampling of the signal in a time interleaved fashion subsequently splitting the data stream into two channels (A and B). This is essential for reducing of the effective data rate necessary to relax timing requirements for further signal processing. The Viterbi decoder consists of an Add-Compare-Select (ACS) function and a Survival Sequence Register (SSR). A 2:1 MUX assembles the error corrected data back into a single bit stream and ships it out through a 50 $\Omega$  terminated buffer. The Clock Recovery (CR) block provides the timing for the FIR, ACS and SSR as well as the synchronization of the other on-chip functions.

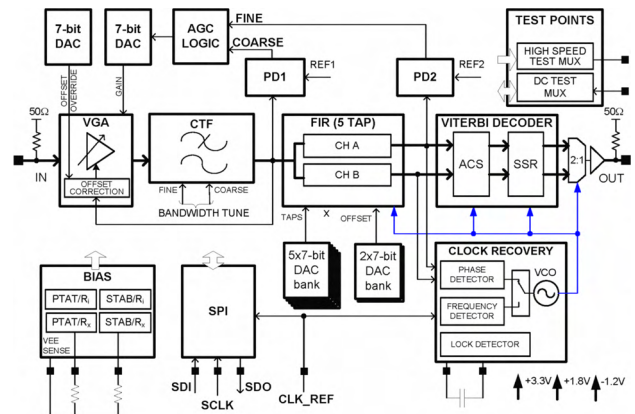


Figure 1. Analog PRML receiver IC architecture.

The Automatic Gain Control (AGC) loop involving the VGA, Peak Detectors (PD) and an AGC logic block is responsible for coarse tuning of the CTF output signal swing. When the CR enters the phase locked mode, the AGC control logic switches to the “fine” loop through the PD2 maintaining the signal swing at the FIR (Ch A) output equal to REF2. The VGA gain in the AGC loop is controlled by a 7-bit DAC. An automatic offset correction feature is employed for canceling out of the offset introduced in the VGA and the CTF. An offset control overriding option is implemented in order to provide for external offset control. For example, it allows the Forward Error Correction (FEC) processor to optimize the offset based on the minimum bit error rate. PTAT and Band-Gap bias currents referenced to internal as well as external resistors are generated for various analog functions. High-speed as well as DC test functions are implemented in order to make possible probing of the signals along the data

path as well as DC bias voltages and also temperature in three different on-chip locations.

### A. VGA/AGC

A linear VGA (Fig. 2) is implemented as a part of a dual loop AGC normalizing the signal amplitude at the FIR input (coarse loop) and at the FIR output (fine loop). The gain (from -8dB to +4dB) is controlled by a current from a 7-bit DAC. Thermometer coding is used in the DAC in order to ensure monotonic transfer characteristic for avoiding of the AGC loop malfunction. The DAC is controlled by the AGC logic block which functions according to a special algorithm. The gain control loops are working one at a time. The coarse loop lock is achieved first. It ensures that a 900mVpp swing data signal enters the FIR. Once the CR achieves a lock condition, the coarse loop is switched off transferring the control to the fine loop for continued monitoring and fine adjustment of the data signal swing at the output of the FIR. The fine loop is also responsible for the accommodation of any deviations of the signal level at the output of TIA during the operation of the IC. The automatic offset control block cancels out any offset in the signal chain along VGA and the CTF. A Gm-C based loop filter instead of an RC filter is used for setting the low frequency response of the automatic offset control, since the implementation of the Gm cell requires much less on-chip area compared to Mega-Ohms of resistance necessary for the low cut-off frequency. Moreover, Gm in contrast to R can be set virtually independent on process corners. This is achieved by deriving the Gm cell bias current using an external resistor. Temperature dependence is eliminated by using PTAT bias current. 100Hz low frequency cut-off is achieved. The offset control voltage on the capacitor is converted to current by another Gm cell which is subsequently inserted into the VGA output termination point. This ensures the offset control loop bandwidth independence on the VGA gain. The automatic offset control can be disabled for external digital control of the offset through the 7-bit DAC.

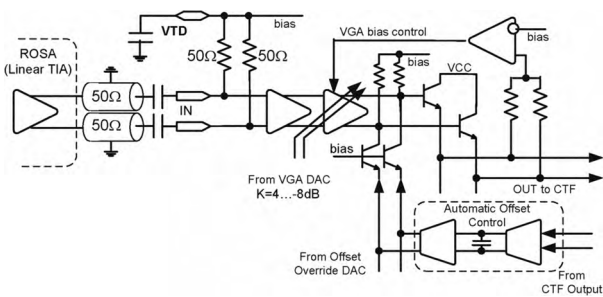


Figure 2. Simplified VGA schematics

### B. CTF

Fig. 3 shows a block diagram of the 4<sup>th</sup> order G<sub>m</sub>-C low-pass CTF. It consists of two bi-Quads, the input voltage-to-current converter and the output current-to-voltage converter. A three bi-Quad version of the filter (6<sup>th</sup> order) has previously been described in detail [4]. This CTF features 230mW – significantly lower power compared to the reported 6<sup>th</sup> Order CTF. The CTF cut-off frequency can be tuned from 1.5 to 3.5 GHz with 4-bit granularity through a digital serial interface. The tuning range is sufficient to

accommodate the incoming data rates ranging from 9.953Gb/s to 11.1Gb/s. Additional 4-bit cut-off frequency tuning capability is built-in for the compensation of the impact on the cut-off frequency of the component parameter variation over process corners. The CTF group delay was measured to be flat to +/- 10ps up to 1.2 times the BW. THD was measured to be below -40dBc at 500MHz frequency.

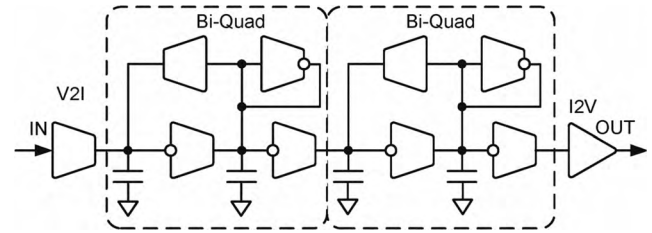


Figure 3. Continuous Time Filter (CTF) block diagram

### C. FIR

The 5-tap sampled-time analog programmable finite impulse response (FIR) filter operates along with the CTF in order to match the combined response of the optical channel and the CTF-FIR to a predefined target – class-2 partial response (PR) polynomial  $(1+D)^2$ . The interleaved FIR is clocked at 5GHz, taking 1 sample per bit of the incoming signal. The linearity and SNDR is 40dBc and 35dBc, respectively, for the entire VGA-CTF-FIR signal chain. The FIR outputs correspond to the 5-level partial response target. A newly developed track-and-hold (T/H) architecture in Fig. 4 achieves >50dBc linearity and >45dB feed-through suppression from a single +3.3V supply by using a switched diode isolation stage in addition to the standard switched emitter follower T/H architecture. A buffer amplifier adds further isolation and restores the gain to unity in order to overcome the losses in the T/H core. The performance of the T/H is critical since any errors or imperfections introduced in the T/Hs are accumulated along the signal chain. A differential peak-to-peak signal swing of about 900mV has been shown to be the optimum for SNDR purposes by trading off noise degradation and signal distortion. A detailed description of the FIR filter has been presented in [6].

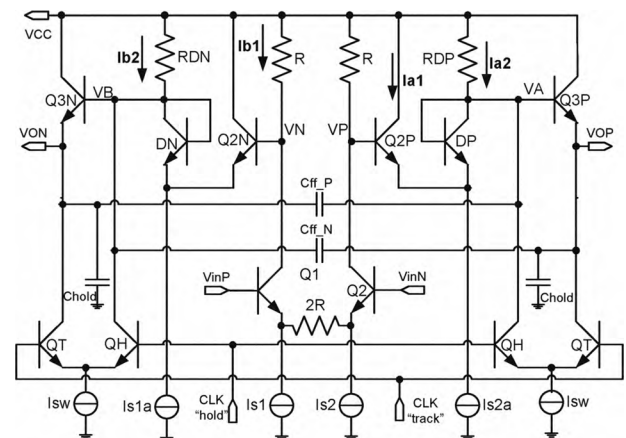


Figure 4. Improved switched emitter follower circuit

### D. Clock Recovery

The clock recovery (CR) uses a decision-directed algorithm approach shown in Fig. 5. Initially, a traditional PLL, with a Phase-Frequency Detector (PFD), has been used to lock the frequency of the Voltage-Controlled Oscillator (VCO) to the incoming data rate. Once frequency lock is achieved, the control of the VCO is transferred to a Decision-Directed Phase Detector (DDPD) phase alignment loop which is using the incoming data stream as reference. The DDPD loop minimizes the Minimum-Mean-Square-Error (MMSE) between the incoming data and the ideal  $(1 + D)^2$  PR2 polynomial. The transition from frequency acquisition mode to phase alignment mode is automatically controlled by a finite-state-machine – the Lock-Detect (LD). Once the LD has been initialized with a reset, the LD will automatically control the dual-loop CR. The CR loop drives the FIR and the Viterbi decoder clock inputs maintaining an optimal sampling phase. A detailed description of the CR has been provided in [5].

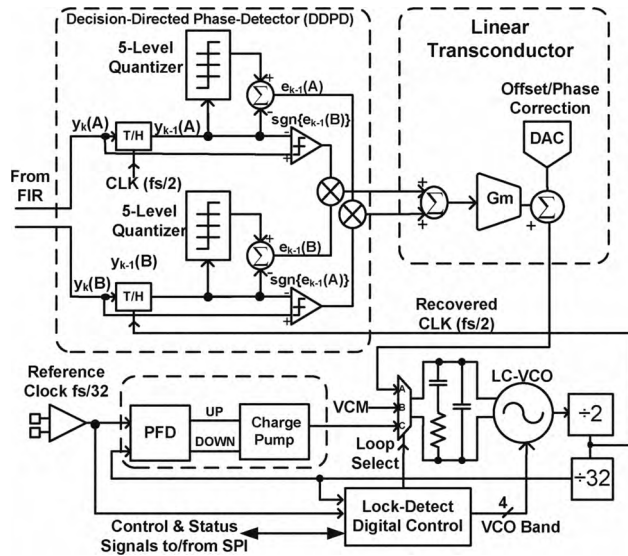


Figure 5. Clock Recovery block functional diagram.

### E. Viterbi Decoder

The interleaved discrete-time analog ACS architecture employs a 4-state MLSE engine to process the PR2, 5-level signals from the FIR (Fig. 6). The ACS is optimized for an  $(1+D)^2$  PR target that is obtained by applying the frequency equalization on the original binary sequence. The two 5-level equalized input signals from the FIR channels A and B are retimed in two track and hold circuits and distributed to the ACS core slices as well as to unity gain linear output buffers connecting to the phase detector block in the CR. Each slice contains an interleaved version of the metric update circuitry, the metric track-and-hold and additional support circuits. The challenge of the non-windowed non-unrolled-loop branch/path metric calculation is the constraint of the extremely short cycle time of under 100ps. From a system point of view, the ACS metrics update equations are uniquely arranged to allow the circuit implementation to achieve the maximum circuit symmetry paired with the maximum SNR at the digital decision circuits. This is vital for achieving the high equivalent input

SNR and low bit error rates. The performance of the ACS block is determined by the accuracy of the internal metric update calculation and the accuracy of the equalization in the CTF/FIR front-end to match the optimum 5-level target. A 2x4-channel digital output of the ACS bus connects to the SSR (Fig. 7) channels: interleave A and B. The SSR block chooses the final survivor based on a majority vote calculation at the end of the SSR chain. The interleaved channels are finally combined in a 2:1 MUX circuit and fed into an XFI compliant output buffer. All SSR clocking is implemented at half-rate. As a result, the residual offset and/or duty cycle distortion in the clock signal driving the output 2:1 MUX can cause even-odd bit duty cycle distortion. Special care was taken to mitigate this effect by providing careful offset compensation for clock driver circuitry.

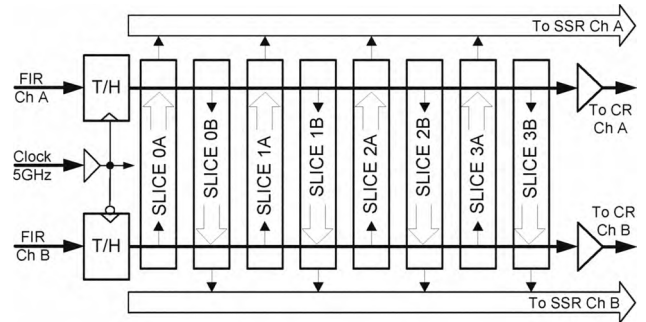


Figure 6. Viterbi Decoder ACS block diagram

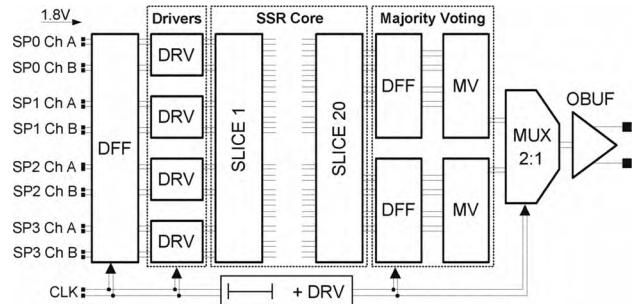


Figure 7. Viterbi Decoder SSR block.

### F. Test Points

The high complexity of this analog receiver makes it difficult to assess the operation of the functional blocks and to identify potential problems in the circuits. High-speed Test Point (TP) circuits are introduced for probing the signals. The use of TP makes it possible to pick up the high speed data signals at the critical points along the signal path with minimal loading of the precision-analog circuits and minimal perturbation of the layout integrity (Fig. 8).

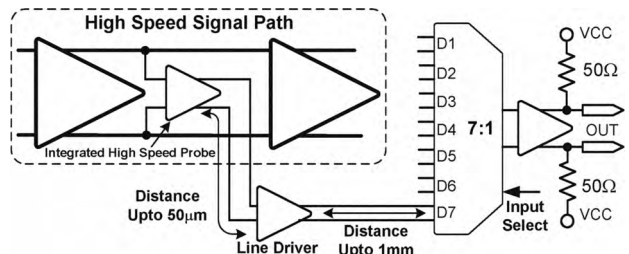


Figure 8. High speed test point implementation

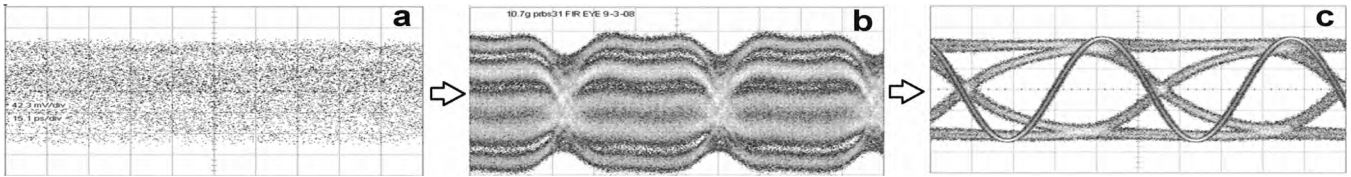


Figure 9. Measured eyes for 400km SMF link: at the receiver input (a), FIR output (b), IC output (c)

A high-speed signal is picked up by a probe that has a driving capability to transmit the signal to the periphery of the block ( $\leq 50\mu\text{m}$ ). A line driver picks up the signal from the probe and transmits it over larger distance ( $\leq 1\text{mm}$ ). An analog MUX selects one out of up to 7 high speed signals coming from the line drivers and ships them to the output through a  $50\Omega$  terminated linear buffer. The DC voltages of the critical biasing points, the voltage drop on ground plane and power supply as well as voltages corresponding to the on-chip temperature are routed out through an integrated DC test point. Since the DC test point is bi-directional it also provides the capability of adding or subtracting of currents to/from a specific point in the circuit.

### III. IC IMPLEMENTATION

A  $0.18\mu\text{m}$  SiGe process is used for the IC implementation. The die size is  $2.5\text{mm} \times 2.5\text{mm}$  (Fig. 10) with the VGA occupying  $0.15\text{mm}^2$ , CTF  $0.17\text{mm}^2$ , FIR  $0.21\text{mm}^2$ , CR  $0.68\text{mm}^2$ , ACS  $0.55\text{mm}^2$ , SSR  $0.14\text{mm}^2$ . The test chip is wire-bonded in a custom ceramic BGA package and consumes  $4.5\text{W}$  from  $3.3\text{V}$ ,  $1.8\text{V}$  and  $-1.2\text{V}$  supplies.

### IV. TEST RESULTS

To assess the performance of the PRML EDC receiver IC, a  $10.71\text{Gb/s}$   $2^{31}-1$  PRBS NRZ data is launched onto an uncompensated  $5 \times 80\text{km}$ -span SMF fiber link. A standard Mach-Zehnder modulator is used. The light source is a  $1550\text{nm}$  wavelength laser, and the link consists of four Erbium-doped fiber amplifiers spaced at  $80\text{km}$ . An optical band-pass filter precedes a standard linear PIN-TIA receiver. A bit-error rate tester was used to detect errors and generate the NRZ data signal. Fig. 9 depicts the received eye after a transmission distance of  $400\text{km}$  (a), the equalized eye at the FIR output (b) and the recovered clock and data eye at the IC output (c). As can be seen, the received eye is totally closed. The PR2 equalization has produced the expected  $(1+D)^2$ , 5-level eye (with residual miss-equalization) which is then applied to the 4-state MLSE for NRZ data recovery. The required back-to-back OSNR is  $16\text{dB}$  and approximately  $25\text{dB}$  at  $400\text{km}$  (i.e.,  $6800\text{ps/nm}$ ). The required OSNR increases at a slope of less than  $1.5\text{dB}/80\text{-km-span}$  (or  $1.5\text{dB}/1360\text{ps/nm}$ ) for the first 3 spans. Over the last two spans, the slope increases to about  $2.5\text{dB}/\text{span}$ .

### V. CONCLUSIONS

The PRML receiver presented here is capable of post-FEC error-free recovery of up to  $11.1\text{Gb/s}$  data transmitted over  $400\text{km}$  of uncompensated SMF fiber. In contrast to existing MLSE receivers that fully rely on a digital Viterbi decoder, our architecture is entirely analog. The realized reach of this receiver exceeds that of any reported EDC receiver employing standard NRZ transmission and direct detection (non-coherent, IM-DD) means (Table I). The

outstanding performance of this PRML receiver has been achieved with a 1-sample/bit, 4-state MLSE [3]. This EDC receiver shifts optical transmission issues from the optical domain to a low cost IC solution. To the best of our knowledge this is the first reported analog implementation of the PRML algorithm for a  $10\text{Gb/s}+$  fiber-optic receiver.

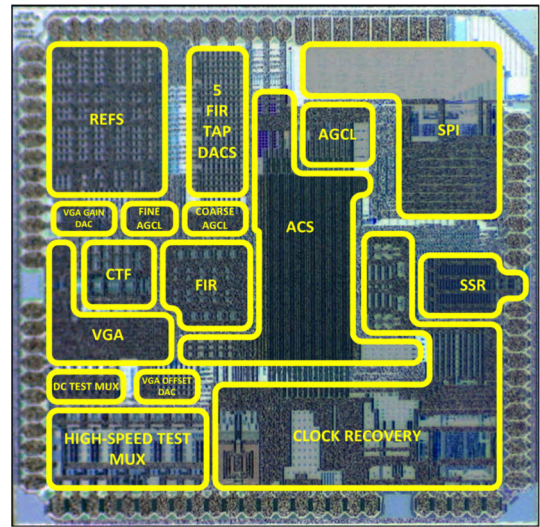


Figure 10. EDC die photo

Table I. Comparison with state-of-the-art solutions

Reference	Number of states	Samples per bit	ADC required	Performance (reach)
[7]	4	2	Yes	120km
[8]	4	2	Yes	160km
[2]	8	1	Yes	300km
Our work	4	1	No	400km

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