Demonstration of a 270 GHz f_T SiGe-C HBT Within a Manufacturing-Proven 0.18µm BiCMOS Process Without the Use of a Raised Extrinsic Base

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ABSTRACT

SiGe bipolar transistors with F_T of 270 GHz are integrated within a standard 0.18 µm CMOS process flow. These devices are built using the same architecture as Jazz' SBC18 SiGe BiCMOS process which has been in high-volume manufacturing for several years. The transistors have an F_{MAX} of 170 GHz but a path to achieving an F_{MAX} equal to F_T is demonstrated without the use of selective SiGe epitaxy or raised extrinsic base poly layers. Data is shown that suggests that the target of 270 GHz F_{MAX} can be achieved through a combination of modest design rule changes and optimization of extrinsic base doping conditions.

INTRODUCTION

In recent years, high performance coupled with low manufacturing costs has enabled SiGe BiCMOS to become the technology of choice for wireless and wireline communications systems. SiGe BiCMOS technologies have enabled devices with F_T and F_{MAX} >300GHz through the use of advanced processing techniques such as selective epitaxy [1] and raised extrinsic base processing techniques [2]. While undoubtedly delivering peak performance, these additional process steps, not ordinarily found in traditional CMOS process flows, may compromise both the manufacturability and cost advantages offered by SiGe BiCMOS technology.

In this paper, we demonstrate SiGe HBTs with F_T of 270 GHz and F_{MAX} of 170 GHz integrated within a current-generation 0.18µm SiGe BiCMOS process flow. This process leverages the learning gained from Jazz' highly manufacturable 0.18µm SiGe BiCMOS technology, SBC18, which has been in high-volume production, delivering thousands of wafers per year, for several years. The new devices are fabricated by aggressively scaling the vertical profile of the current generation devices without adjusting any of the thermal budget or process steps necessary for the parent CMOS process. Then a set of experiments is discussed which seeks to improve F_{MAX} to the point where $F_T = F_{MAX}$. This is to be accomplished by employing only modest design rule and extrinsic base doping optimization without adding any significant process complexity such as selective epitaxy, CMP of NPN layers, or multiple base deposition steps.

EXPERIMENT

The SBC18 technology makes use of a sacrificial emitter post combined with multiple spacer-implant process steps in order to create a fully self aligned (FSA emitter structure [3]. See figure 1 for an illustration of the device. The fastest device currently offered within this integration scheme is a SiGe HBT with F_T=F_{MAX}=200GHz (this specific process variant is called SBC18H2).

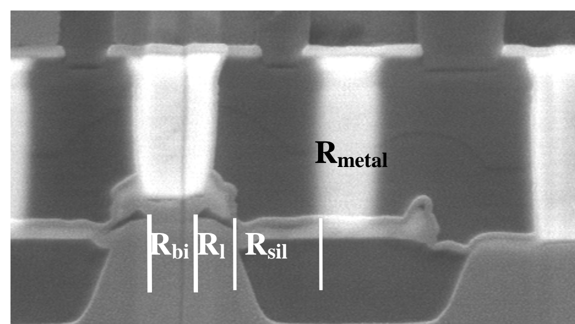

Figure 1: SEM micrograph of an SBC18H2 device with base resistance components illustrated. R_{bi} is the intrinsic "pinched" base resistance underneath the emitter. R_l is the unsilicided "link" resistance underneath the emitter poly overhang, R_{sil} is the silicided extrinsic base resistance and R_{metal} includes all resistances associated with back end metallization.

With further aggressive scaling of the vertical NPN profile, the SBC18H2 device can be accelerated to 270 GHz F_T without any significant process changes. All of the doping levels and physical layer thicknesses used to create the 270 GHz device are well within the realm of standard processing parameters in Jazz' fab. Figure 1 shows Gummel, base current reversal, and output curves for the 270 GHz device. This device had a maximum current gain of about 450, BV_{CEO} of 1.73V, BV_{CBO} of 4V and an Early voltage of 900V.

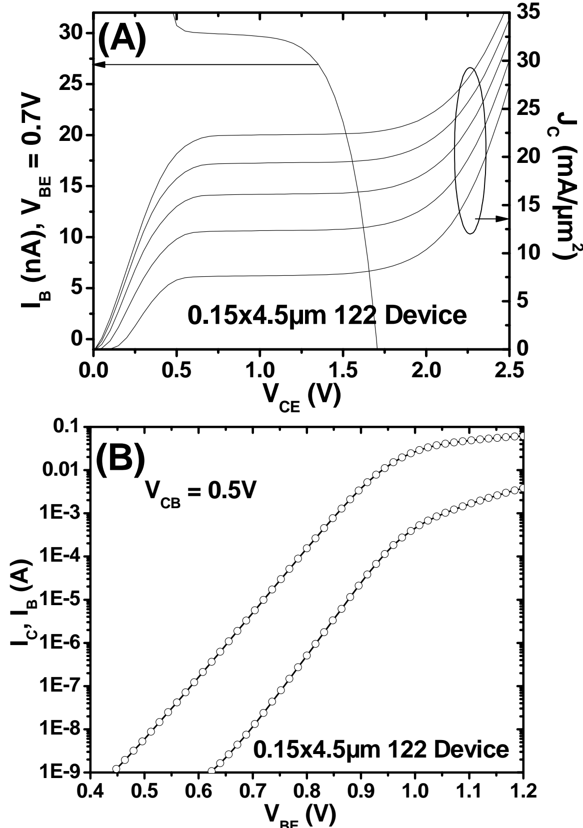

Figure 2: DC characteristics of a 0.15 × 4.5 μm single emitter, double base, double collector HBT with F_T=270 GHz. Figure (A) shows output curves with a base current reversal plot overlaid. Figure (B) shows a Gummel plot taken at V_{CB} = 0.5V

Figure 3 shows the RF characteristics of a 270 GHz device. The highest F_T measured was just over 270 GHz and F_{MAX} of over 180 GHz was measured on shorter devices (2.8μm) but with somewhat lower F_T and slightly noisier data due to the smaller RF signal.

In addition to achieving this high value of F_T within the current process flow, a significant challenge remains in increasing the F_{MAX} to be comparable to F_T without enabling drastic process changes. The purpose of the experiments below is to explore how far F_{MAX} can be pushed within the limitations of the current process; i.e. a single, non-selective base deposition, the present fully self aligned emitter post integration with simple oxide outer spacers (no "inside" or nitride/oxide spacers) and traditional device layout.

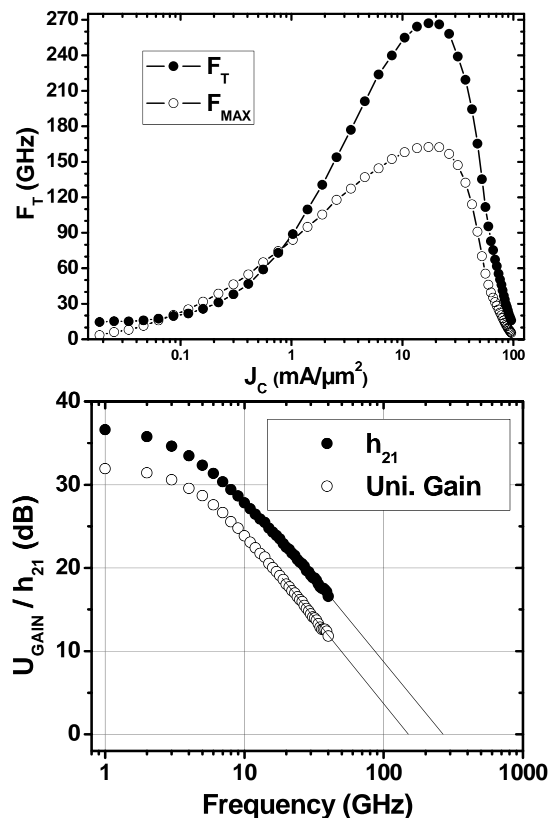

Figure 3: RF characteristics of a 0.15 × 4.5μm single emitter, double base, double collector HBT. Figure (A) shows F_T and F_{MAX} vs. J_C with V_{CB} held at 0.6V. Figure (B) shows h_{21} and unilateral gain vs. frequency for bias conditions near that of the peak in figure (A)

In order to improve F_{MAX} without sacrificing F_T one needs to find ways to improve the base resistance and collector base capacitance without compromising the vertical profile or the DC characteristics.

The total base resistance consists of 4 components as shown in figure 1. The intrinsic base region directly underneath the diffused emitter has the highest sheet resistance of any of the base resistance components. Vertical scaling to improve F_T is usually accompanied

by a shrink of the emitter width in order to compensate for the higher intrinsic base sheet resistance. In the case of the 270 GHz device shown above, the F_T / F_{MAX}^2 metric is equal to 9.3ps. It would need to be improved to 3.7 ps in order to achieve $F_T = F_{MAX}$. Brute force scaling of the emitter would thus require a 60nm emitter width which is not yet feasible under our current lithography capabilities. For this study it will be assumed that only a modest shrink from the current 0.15µm (as measured by cross sectional SEM) emitter width can be achieved. The rest of the F_{MAX} improvement must come from optimization of the extrinsic base regions. After other avenues of base resistance optimization have been exhausted the emitter width will be reevaluated to determine the necessary shrink to obtain a device with $F_T = F_{MAX}$.

The first set of experiments intended to improve the extrinsic base resistance focuses around process improvements. Extrinsic base implant conditions were optimized by varying the dose, energy and species of the multiple extrinsic base implants. The order of the implants in the process as well as spacer widths and types were examined. Figure 4 shows box plots of F_{MAX} and extracted $R_B \times C_{BC}$ product for devices with various extrinsic base process splits. The dashed lines in the $R_B \times C_{BC}$ plot show where the 270 GHz device lies and the value needed to reach 270 GHz F_{MAX}.

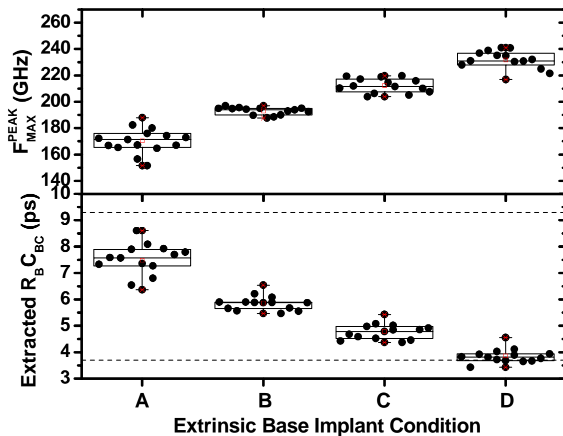

Figure 4: Box plots of F_{MAX} and extracted $R_B \times C_{BC}$ for devices with various extrinsic base improvements. The dashed lines represent the $R_B \times C_{BC}$ product for the 270 GHz device (9.3ps) and where it needs to be to achieve 270 GHz F_{MAX} (3.7ps)

The dramatic improvement in F_{MAX} with only a slight deterioration of F_T is due to a reduction in extrinsic base sheet resistance. In particular, the activation of dopant species for a given implant dose was greatly improved while using the same thermal cycles as the current process.

Most extrinsic base improvements trade off with emitter base leakage at low V_{BE} or BV_{CBO}. In the case of these improvements neither parameter was degraded significantly. Figure 5 shows scatter plots of F_{MAX} vs. BV_{CBO} and vs. I_B at V_{BE} = 0.4V. It can be seen that there is a clear correlation between F_{MAX} and BV_{CBO} but basically none with I_B leakage. So the limitations to these process improvements are a slight deterioration in F_T and BV_{CBO}. A conservative estimate for the amount of $R_B \times C_{BC}$ improvement due to these process improvements is 33%.

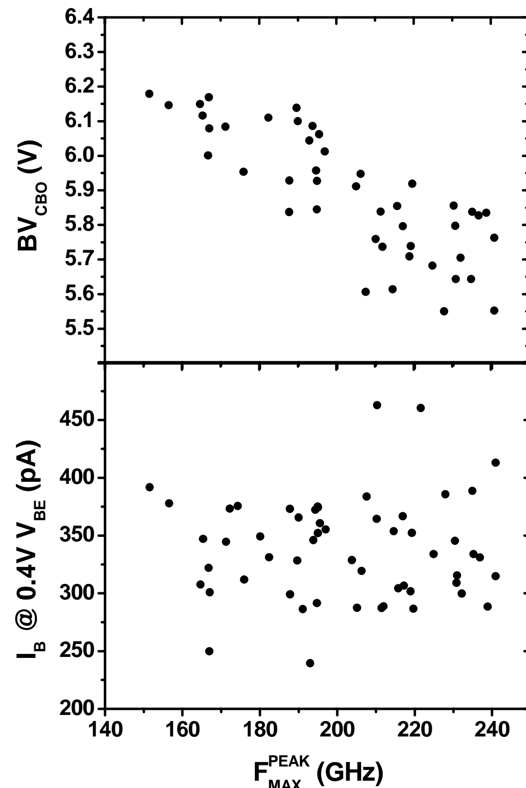

Figure 5: Scatter plots of F_{MAX} vs. BV_{CBO} and vs. I_B at V_{BE} = 0.4 V for devices with various extrinsic base process improvements.

The second set of experiments focuses on design rule optimization. Again, the rules were varied under the constraint that the line widths and overlay tolerances must be comfortably within the capabilities of Jazz' current toolset.

Figure 5 shows box plots of F_{MAX} and extracted $R_B \times C_{BC}$ product for devices with various active design rule optimizations.

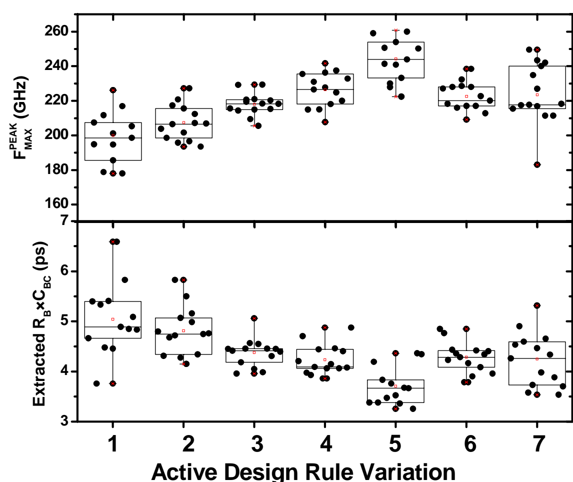

Figure 6: Box plots of F_{MAX} and $R_B \times C_{BC}$ for devices with varying active design rules.

The improvements with active design rule are not necessarily just due to simple reduction of C_{BC}. For the silicided-extrinsic base devices examined here, active sizing also plays a role in determining R_B and thus the active size and active overplot of emitter rules need to be carefully optimized (not just minimized) to optimize F_{MAX}. An estimate of the $R_B \times C_{BC}$ improvement for the optimal active design rules relative to the current process is 25%.

The overplot of the emitter poly over the emitter window is an extremely important parameter for reducing F_{MAX} for silicided extrinsic base devices since the overplot essentially determines the length of R_l from figure 1; the unsilicided, implanted extrinsic base poly/epi. However it is much more challenging from a process point of view to reduce this dimension than to effect the active design rule changes discussed above. Nevertheless a modest reduction in emitter poly design rule is acceptable for a leading edge process such as this. A scatter plot of F_T vs. F_{MAX} for emitter poly design rule changes is shown in figure 7. The tradeoff with reducing the emitter poly overplot is with emitter base leakage due to implant damage, transient enhanced diffusion or simply the proximity of a highly doped p-type region laterally close to the emitter base junction. Due to these risks, an estimate of the available $R_B \times C_{BC}$ improvement from EP design rule improvements is only about 10%.

Using the process and layout improvements discussed above and the conservative estimates for $R_B \times C_{BC}$ reduction due to those improvements it is estimated that the $R_B \times C_{BC}$ of the 270 GHz F_T device shown above could be reduced from 9.3 ps to 4.2 ps leading to an F_{MAX} of 253 GHz. The remaining improvement would have to come from scaling of the emitter itself. After the extrinsic base improvements and the slight increase of R_{bi} in creating the 270 GHz device relative to a 200 GHz device, the intrinsic base resistance contributes closer to 75% of the total. Thus the emitter would need to shrink by 15% to meet the final goal of 3.7ps. This corresponds to a final emitter width of just under 0.13µm which is within current manufacturing capabilities.

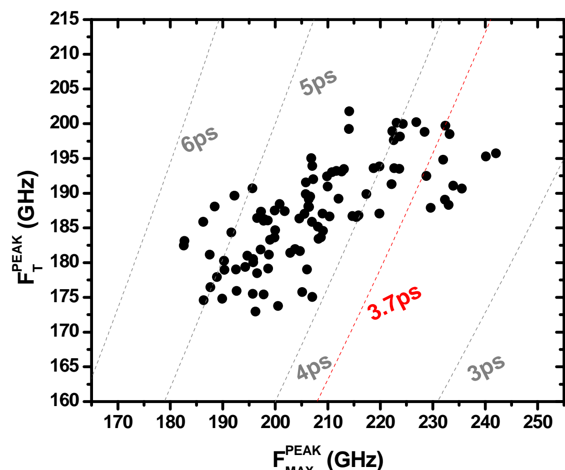

Figure 7: F_T vs. F_{MAX} scatter plot for devices with varying emitter poly design rules. The dashed lines are lines of constant $R_B \times C_{BC}$.

CONCLUSION

A SiGe HBT with F_T of 270 GHz is demonstrated within a process capable of volume manufacturing as proven by several years and tens of thousands of wafers produced in Jazz' fab. In order to improve F_{MAX} of this device to be equal to F_T, several improvements in process and design rule optimization are presented which drastically reduce extrinsic base resistance without compromising other device figures of merit or manufacturability. Finally an emitter width shrink down to 0.13 µm will enable a matched 270 GHz F_T / F_{MAX} device.

REFERENCES

[1] P. Chevalier et al., *Proc. 2005 BCTM*, p. 120.
[2] B. Orner et al., *Proc. 2006 BCTM,* p. 49.
[3] M. Racanelli et al., *Proc. 2001 IEDM*, p. 336.