Benchmark Tests for MOSFET Compact Models With Application to the PSP Model

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***Abstract*—This paper presents the results of several qualitative "benchmark" tests that were used to verify the physical behavior of the PSP model and its usefulness for future generations of CMOS IC design. These include newly developed tests and new experimental data stemming from low-power, RF, mixed-signal, and analog applications of MOSFETs.**

***Index Terms*—Benchmark tests, compact model, MOSFET, surface-potential-based model.**

I. Introduction

COMPACT MOSFET models should both provide an accurate reproduction of the minute details of transistor behavior (e.g., higher order transconductances) and be computationally efficient. The latter inevitably requires the use of empirical relations or approximations. By using the surface-potential-based approach to compact modeling [1], the physics content of a compact MOSFET model significantly increases, but the use of semiempirical relations cannot be completely eliminated. It is therefore necessary to prevent unphysical behavior of a compact model, which can occur as an unintended consequence of the use of empirical relations or approximations [2]. Over the years, two techniques have proven to be particularly useful for assuring the high quality of compact models. The principle of asymptotic correctness [3] essentially states that even empirical equations should become exact in extreme cases. This concept has been extensively used in the development and formulation of PSP. In addition, several "benchmark tests" have been formulated to address those aspects of the qualitative behavior of compact models that are of particular interest to circuit designers [4]–[6]. In this paper, we demonstrate that the new industry standard PSP model satisfies the traditional tests [4]–[6], and we introduce several new tests that verify that PSP meets the stringent requirements imposed on compact models by the continued scaling of MOS devices and their widespread use in RF applications. In this paper, we concentrate on dc and ac tests.

Benchmarking of PSP has been already reported in [7]. In the present investigation, we include additional theoretical results for the traditional tests, analysis of the relation between the singularity at $V_{\rm ds} = 0$ and harmonic balance simulation results, and some results for benchmarking of the PSP-SOI model. We also expand the investigation of the nonreciprocity of transcapacitances at $V_{\rm ds} = 0$ as it relates to the charge-sheet approximation.

The qualitative behavior of PSP does not depend on parameter values. The only exception concerns the strict requirement of the existence of the fifth derivative at $V_{\rm ds} = 0$ that is discussed in Section III-B. For this reason, and to make the results of this work easily reproducible, we have used default parameters in most simulations. However, for the experimental verification of high-order derivatives at $V_{\rm ds} = 0$, we have used PSP parameters for the Jazz Semiconductor 0.18-μm process (cf. Section II-D).

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II. Traditional Benchmark Tests

Among the most important traditional benchmark tests are the slope-ratio (Fig. 1) and tree-top tests (Fig. 4), which evaluate the subthreshold $V_{\rm ds}$ behavior and the g_m/I_d ratio behavior of a model, respectively [6]. These tests essentially require the qualitative behavior of a model to be similar to that of the Pao–Sah [8] or charge-sheet model [9]. Since PSP is a direct descendant of these models, it easily passes both tests for all model parameter values.

A. Slope-Ratio Test

The purpose of the slope-ratio test is to confirm that a MOSFET model can distinguish the qualitative difference in $I_{\rm ds}(V_{\rm ds})$ behavior between subthreshold and strong inversion

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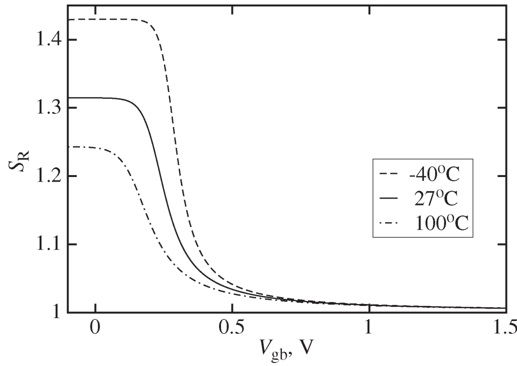

Fig. 1. Traditional slope-ratio test results for PSP using default parameters with $W/L = 10/10$ μm for different temperatures; $V_{\rm db1} = 10$ mV, $V_{\rm db2} = 20$ mV, and $V_{\rm sb} = 0$.

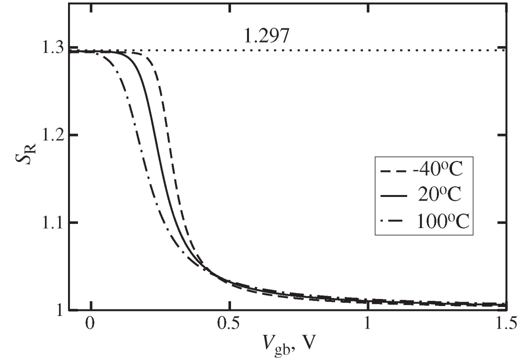

Fig. 2. Modified temperature-independent slope-ratio test results for PSP with default parameters; $\Delta V = 1$ mV.

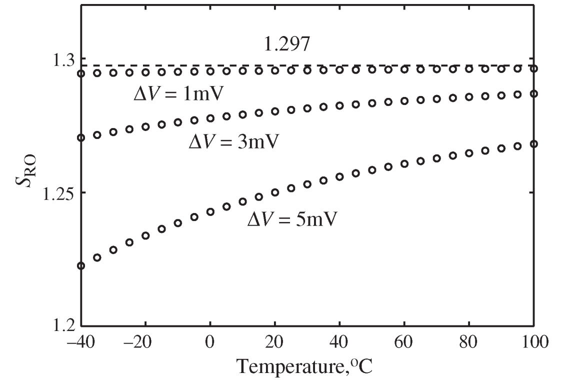

Fig. 3. Sensitivity of $S_{\rm RO}$ to ΔV for PSP.

operation. This is verified by the reduction of the slope ratio from about 1.3 to 1 with the increase of the gate bias.

The slope ratio is defined as

$$S_R = \frac{(I_2 + I_1)(V_{\rm db2} - V_{\rm db1})}{(I_2 - I_1)(V_{\rm db2} + V_{\rm db1})} \tag{1}$$

where I_1 and I_2 are the drain currents corresponding to $V_{\rm db} = V_{\rm db1}$ and $V_{\rm db} = V_{\rm db2}$, respectively. Fig. 1 shows that PSP passes the test with commonly used $V_{\rm db1} = 0.01$ V and $V_{\rm db2} = 0.02$ V. The traditional version of the slope-ratio test (1) suffers from a temperature dependence of the limiting value $S_{\rm RO}$ of S_R in subthreshold region (see Fig. 1). Indeed, the subthreshold current can be expressed as [8]

$$I_d = \mu \frac{W}{L} C_{\rm ox} \cdot \frac{\gamma \phi_t^2}{2\sqrt{\phi_{\rm ss}}} e^{(\phi_{\rm ss} - 2\phi_B - V_{\rm sb})/\phi_t} \left(1 - e^{-V_{\rm ds}/\phi_t}\right) \tag{2}$$

where μ is the mobility, $C_{\rm ox}$ is the oxide capacitance per unit area, γ is the body effect factor, $\phi_{\rm ss}$ is the surface potential at the source end of the channel, ϕ_B is the "Fermi potential," and $\phi_t = k_B T/q$ is the "thermal potential." Then

$$S_{\rm RO} = \frac{e^{\beta V} - \cosh(\beta \Delta V)}{\sinh(\beta \Delta V)} \cdot \frac{\Delta V}{V} \tag{3}$$

where

$$\beta = 1/\phi_t \tag{4}$$

$$V = \frac{V_{\rm db1} + V_{\rm db2}}{2} \tag{5}$$

$$\Delta V = \frac{V_{\rm db2} - V_{\rm db1}}{2}. \tag{6}$$

As long as $V_{\rm db1}$ and $V_{\rm db2}$ are fixed (i.e., temperature independent), βV and $\beta \Delta V$ depend on temperature, producing the results shown in Fig. 1. In addition to the $S_{\rm RO}$ temperature dependence, it is not clear what the correct (or ideal) value of $S_{\rm RO}$ is, even at room temperature. To remedy this problem, we select

$$V_{\rm db1} = \frac{\phi_t}{2} - \Delta V \tag{7}$$

$$V_{\rm db2} = \frac{\phi_t}{2} + \Delta V \tag{8}$$

where $\Delta V \ll \phi_t$. Then, $V_{\rm db1} + V_{\rm db2} = \phi_t$, and from (3)

$$S_{\rm RO} = 2\left(\sqrt{e} - 1\right) \approx 1.297 \tag{9}$$

regardless of the temperature. Typical results for PSP are shown in Fig. 2 for $\Delta V = 1$ mV, while the sensitivity of $S_{\rm RO}$ to the magnitude of ΔV is shown in Fig. 3. Just as for the original version, the proposed modification of the slope-ratio test checks the conformance of a compact MOSFET model to the classical behavior (2) in the subthreshold region and is applicable to any model.

B. Tree-Top Test

The purpose of the tree-top test is to assure that the details of g_m/I_d ratio bias dependence relevant to the analog design are accurately reproduced by a MOSFET model. For the tree-top test (cf. Fig. 4), note that, in the subthreshold region from (2)

$$\frac{g_m}{I_d} = \left(\beta - \frac{1}{2\phi_{\rm ss}}\right) \frac{\partial \phi_{\rm ss}}{\partial V_{\rm gs}} \tag{10}$$

or, equivalently

$$\frac{g_m}{I_d} = \left(\beta - \frac{1}{2\phi_{\rm ss}}\right) \left(1 - \frac{C_{\rm gg}}{C_{\rm ox}}\right) \tag{11}$$

where β is defined in (4). The increase of the g_m/I_d ratio with gate bias follows the corresponding decrease of $C_{\rm gg}$. Note also that, as shown in Fig. 4, this ratio never actually reaches

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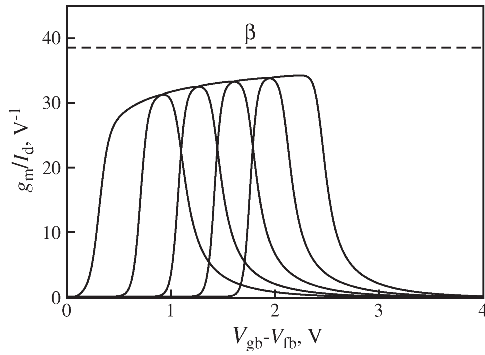

Fig. 4. Tree-top test results for PSP using default parameters with $V_{\rm ds} =$ 50 mV, $V_{\rm bs}$ varies from -1 to 0.2 V in 0.3-V steps, $V_{\rm fb} = -1$ V, $W/L =$ 10/10 μm, and $T = 27$ °C. Horizontal line represents $\beta = 38.6$ V^{-1}.

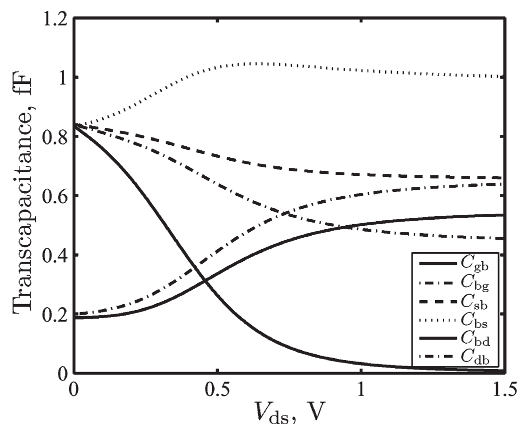

Fig. 5. Transcapacitances for PSP with $W/L = 10/0.08$ μm and $V_{\rm gs} = 1.2$ V.

its theoretical maximum value β since $C_{\rm gg} > 0$. In simpler threshold-voltage-based models, the subthreshold region is often described using the semiempirical relation

$$I_d \propto \exp\left(\frac{V_{\rm gb} - V_t}{n\phi_t}\right) \tag{12}$$

where V_t denotes the threshold voltage, and n is a fixed constant. In this approach

$$\frac{g_m}{I_d} = \frac{\beta}{n} \tag{13}$$

is constant in the subthreshold region, and the effect of the variation of $C_{\rm gg}$ with $V_{\rm gb}$ is lost.

C. Transcapacitances

Transcapacitances as functions of the terminal bias with fine resolution are traditionally investigated to detect possible singular behavior. Fig. 5 shows the typical results that verify the continuous and physical behavior of the transcapacitances of PSP, including the correct sign for $C_{\rm bd}$ and $C_{\rm gb}$. The latter is problematic in some older models that separate charge and current submodels, but in PSP, the symmetric linearization technique [1] provides consistency of both submodels with the desired behavior seen in Fig. 5.

D. GST

The design of certain circuits, most importantly of passive RF mixers and transfer gates, requires symmetry of a MOSFET model with respect to source–drain terminal interchange [10]. The typical results for PSP are presented as solid lines in Fig. 6, indicating that PSP passes this test. As in [6], V_b denotes the body bias, $V_x = V_{\rm ds}/2$, and $V_{\rm bo} = (V_{\rm db} + V_{\rm sb})/2$. Three necessary conditions for this include a nonsingular velocity saturation model [1], [10], an odd smoothing function describing the transition from the triode to the saturation region of the MOSFET characteristics [1], [11], and the symmetry of the linearization procedure for the inversion and bulk charges as functions of the surface potential [1]. The aforementioned discussion refers exclusively to the qualitative behavior of the drain current and its derivatives for $V_{\rm ds} = 0$ (i.e., for $V_X = 0$ in terms of the Gummel symmetry test (GST) setup as in [6]). The results shown in Fig. 6 demonstrate that PSP accurately reproduces the actual test data (symbols). Note that this is the first ever experimental investigation of the higher order derivatives for a MOS transistor operated at zero drain bias and that, only a short time ago, it was impossible to model even the second derivative for $V_X = 0$ with the industry standard MOSFET model.

III. NEW TESTS

A. Subthreshold Region

The purpose of the new test is essentially the same as that of the slope-ratio test—to verify the characteristics of $I_d(V_{\rm ds})$ dependence predicted by (2). The difference is that, instead of the somewhat unintuitive concept of a slope ratio, the test is formulated in terms of output conductance, which is more relevant to both model parameter extraction and design applications. In terms of the output conductance $g_{\rm ds} = \partial I_d/\partial V_d$, we find from (2) that

$$(\partial/\partial V_d)\left[g_{\rm ds} \cdot \exp(V_{\rm ds}/\phi_t)\right] = 0 \tag{14}$$

implying zero slope for $g_{\rm ds} \cdot \exp(V_{\rm ds}/\phi_t)$ versus $V_{\rm ds}$ plots. This is indeed observed in subthreshold operation, while increasing the gate bias leads to the formation of an inversion layer and, consequently, to a finite slope (see Fig. 7). There is an interesting connection between this characteristic behavior and the GST. It is common knowledge that, when velocity saturation is directly included into the charge-sheet MOSFET model, it gives an unacceptable negative $g_{\rm ds}$ in the saturation region. This problem is usually solved via the use of certain smoothing functions to model the transition from triode to saturation region operation by changing $V_{\rm ds}$ into an effective drain bias $V_{\rm dse}$ [1]. To pass the GST, the $V_{\rm dse}(V_{\rm ds})$ function has to be odd [11] with an additional requirement of unity slope at $V_{\rm ds} = 0$ suggested in [12]. In fact, this latter condition is not required for passing the GST but is useful to ensure that (14) is satisfied. More precisely, one needs to require approximately a unity slope of $dV_{\rm dse}/dV_{\rm ds}$ for $V_{\rm ds} < 3\phi_t$. If this condition is violated, so is (14), as shown in Fig. 8.

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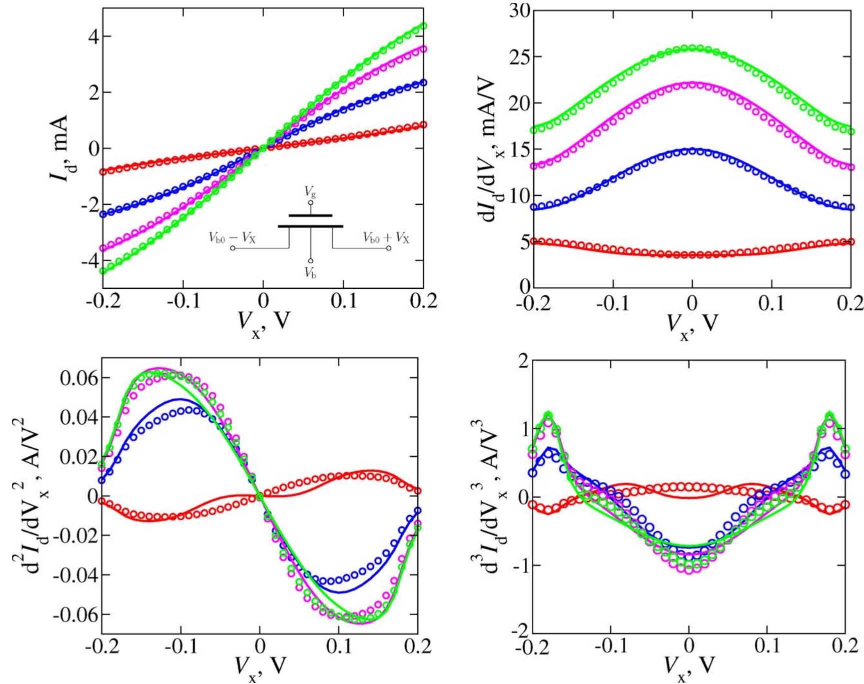

Fig. 6. Drain current and derivatives for Jazz Semiconductor 0.18-μm technology n-channel 10/0.18 μm MOSFET; V_g varies from 0.6 to 1.8 V in steps of 0.4 V. Symbols represent experimental data, while solid lines refer to PSP; $V_b = 0$ V; and $V_{\text{bo}} = 0$ V. Inset shows the circuit diagram for simulation.

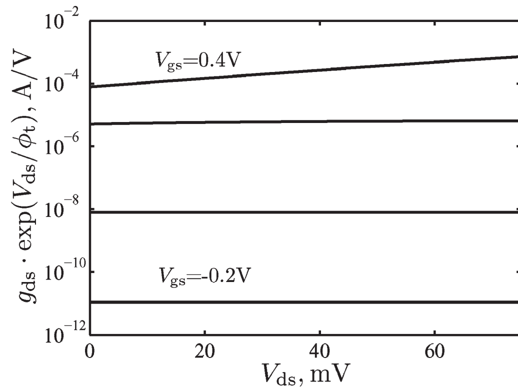

Fig. 7. PSP results for subthreshold region; V_{gs} varies from -0.2 to 0.4 V in 0.2-V steps. Default parameters are used.

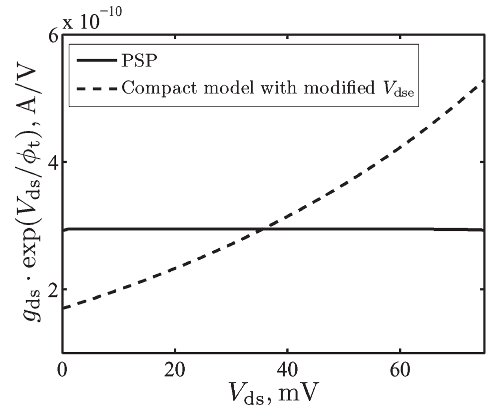

Fig. 8. Comparison of PSP and another compact model with modified V_{dse} for which $dV_{\text{dse}}/dV_{\text{ds}}$ differs from one appreciably for $V_{\text{ds}} < 3\phi_t$; $V_{\text{gs}} = -0.1$ V.

B. Higher Order Derivatives in the GST

To model harmonic distortion in RF circuits operating with zero drain–source dc bias, it is now deemed necessary for compact models to be not just class $C^{(3)}$ (derivatives continuous to third order) but, at least, class $C^{(5)}$. The nature of the smoothing function

$$V_{\text{dse}} = \frac{V_{\text{ds}}}{\left[1 + \left(\frac{|V_{\text{ds}}|}{V_{\text{dsat}}}\right)^{\mathbf{AX}}\right]^{\frac{1}{\mathbf{AX}}}} \tag{15}$$

used in PSP is such that class $C^{(3)}$ behavior is automatically guaranteed ($\mathbf{AX} > 2$), but in order for the nth derivative to exist at $V_{\text{ds}} = 0$, it is necessary to impose the condition

$$\mathbf{AX} > n - 1. \tag{16}$$

One exception to this requirement is when $\mathbf{AX}$ is an even integer in which case the derivatives of all orders exist.

The local parameter $\mathbf{AX}$ scales with the device effective channel length L as

$$\frac{\mathbf{AXO}}{1 + \mathbf{AXL}/L} \tag{17}$$

where $\mathbf{AXL}$ is a global (scaling) parameter. For short-channel devices, this limits the range of $\mathbf{AXL}$, making it more difficult to cfit g_{ds} as a function of drain bias. Typical results for $n = 5$ for different values of $\mathbf{AX}$ are shown in Fig. 9. This limitation is not specific to PSP, and in fact, in the previous standard model, the second derivative does not exist for $V_{\text{ds}} = 0$ [12].

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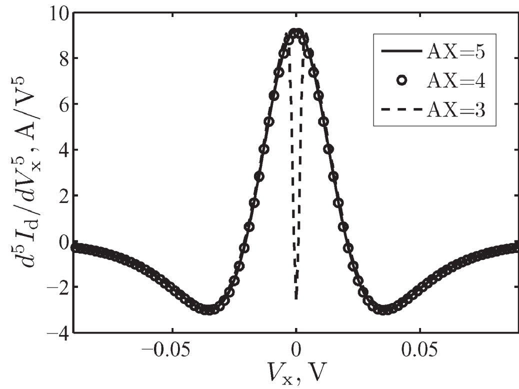

Fig. 9. Fifth order derivatives for different $\mathbf{AX}$ (using the GST biasing scheme). For $\mathbf{AX} = 3$, condition (16) is violated. Apart from $\mathbf{AX}$, PSP model parameters used are for a 90-nm technology node.

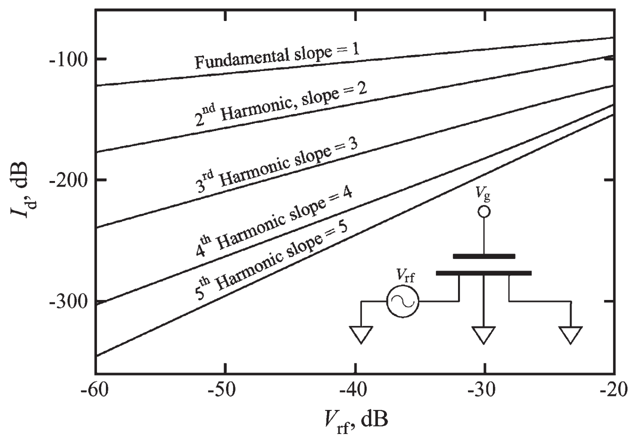

Fig. 10. Single tone harmonic balance simulation result for PSP; $V_g = 0.4$ V, $W/L = 10/0.35$ μm, and fundamental frequency is 100 MHz. Inset shows the circuit diagram for simulation. Default parameters are used for PSP.

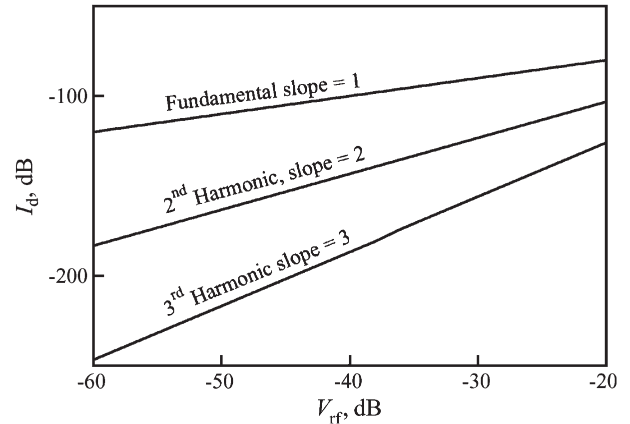

Fig. 11. Single tone harmonic balance simulation results for PSP-SOI; $V_g = 0.5$ V, $W/L = 10/0.5$ μm, and fundamental frequency is 100 MHz. Default parameters are used.

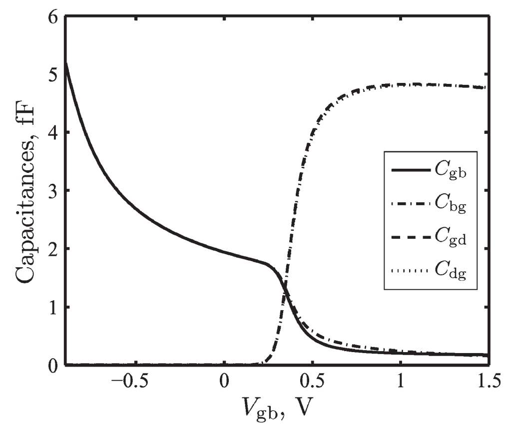

Fig. 12. Transcapacitances C_{gd}, C_{dg}, C_{gb}, and C_{bg} for PSP with $W/L = 10/0.08$ μm at $V_{ds} = 0$. Default parameters are used.

C. Modified Symmetry Test

The traditional GST does not apply in the presence of gate and substrate currents. For this reason, a new test has been developed in [13]. Typical results including gate current presented in [13] and [7] show that PSP passes this test. The last reference also contains the results for SOI MOSFET model with the valence-band tunneling current included [16], indicating that PSP-SOI [14] also passes the test.

D. Harmonic Balance Simulation

Distortion analysis is a key to evaluate the performance of RF circuits. Traditional MOSFET models produce unphysical harmonic balance simulation results for the third and higher order harmonics due to their asymmetric behavior around $V_{ds} = 0$ [10], [18]. A detailed analysis of the origin of this unphysical behavior is presented in the Appendix. Theory [15] indicates that the second harmonic should be proportional to the square of the input signal level, the third harmonic should be proportional to the cube of the input signal level, and so on. Fig. 10 shows a single tone harmonic balance simulation result for PSP using the circuit in Fig. 10. PSP produces correct slopes for up to the fifth order harmonic. Harmonic balance simulation with the PSP-SOI model [16] using a similar circuit was also performed. The results shown in Fig. 11 verify that PSP-SOI has the same qualitatively correct behavior as PSP.

E. Reciprocity

Generally speaking, MOSFET transcapacitances are nonreciprocal. However, for $V_{ds} = 0$ (a condition often used for model parameter extraction), reciprocity is recovered. In both PSP and one of its predecessors MM11 [17], the reciprocity condition is approximately satisfied for $V_{ds} = 0$ with an accuracy sufficient for engineering applications (Fig. 12). Note that the symmetry of the model assures that, in PSP, $C_{ds} = C_{sd}$ exactly for $V_{ds} = 0$.

The small deviation from reciprocity is associated with the charge-sheet approximation [17]. To demonstrate this explicitly, we compare the results of a charge-sheet model [9] with those of the Pao–Sah model [8]. As Fig. 13 shows, the latter satisfies the reciprocity conditions perfectly, while the charge-sheet model has a small nonreciprocity comparable to that of PSP (see Fig. 12), which also uses the charge-sheet approximation.

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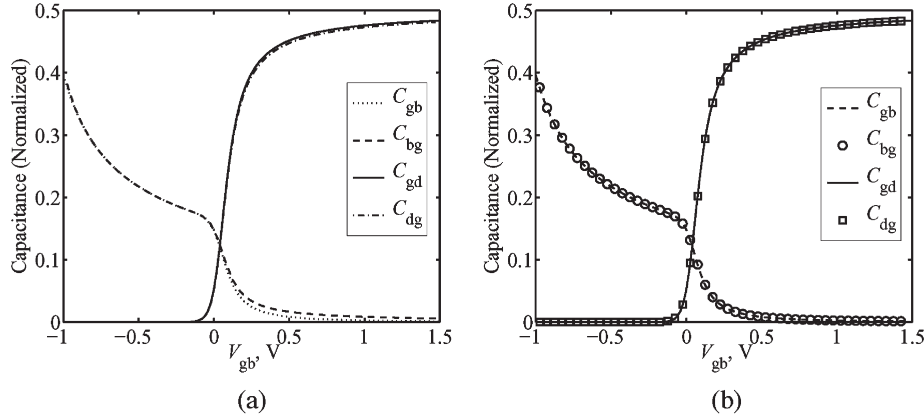

Fig. 13. Transcapacitances $C_{\rm gd}$, $C_{\rm dg}$, $C_{\rm gb}$, and $C_{\rm bg}$ for charge-sheet model [9] and Pao–Sah model [8] at $V_{\rm ds} = 0$, respectively; $t_{\rm ox} = 4$ nm, and $N_a =$ 3E23 m^{-3}. (a) Charge-sheet model. (b) Pao–Sah model.

IV. Conclusion

A battery of traditional, modified, and newly developed benchmark tests is available to MOSFET model developers to evaluate the correct qualitative behavior of compact models. We present the results of the application of these tests to the new industry standard MOSFET model PSP. The experimental data for higher order derivatives of the drain current at $V_{\rm ds} = 0$ are presented for the first time and are accurately reproduced by PSP.

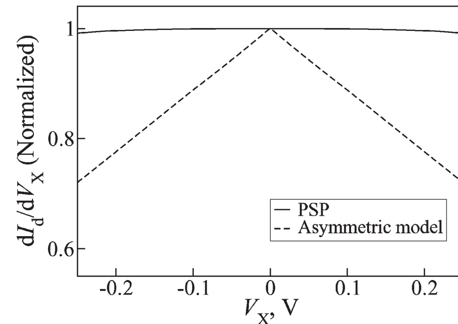

Fig. 14. Illustration of (21) and (25). For PSP $b = 0$, for an asymmetric model, $b = -b' \neq 0$.

Appendix

The origin of the 2 dB/dB slope of the third harmonic characteristics for singular transistor models has been investigated in [18] for a simple MESFET model, keeping second order terms in the analysis. Here, we extend the method of [18] to a more general case and factor in details of how MOSFET models are implemented in circuit simulators.

The implementation of MOSFET models in circuit simulators is such that, regardless of the internal symmetry of a model, the condition

$$I_d = f(V_{\rm sb}, V_{\rm db}, V_{\rm gb}) = -f(V_{\rm db}, V_{\rm sb}, V_{\rm gb}) \tag{18}$$

is imposed. In the case of GST (cf. Fig. 6), V_g and $V_{\rm bo}$ are fixed, and the "symmetry condition" takes the form

$$I_d(-V_X) = -I_d(V_X) \tag{19}$$

where

$$I_d(V_X) = f(-V_{\rm bo} - V_X, -V_{\rm bo} + V_X, V_{\rm gb}). \tag{20}$$

If a compact MOSFET model is inherently symmetric, the imposition of the symmetry condition (18) by the circuit simulator is inconsequential. However, its imposition on asymmetric models produces singularities, usually in the form of the nonexistence of the second derivative d^2I_d/dV_X^2 for $V_X = 0$ (cf. Fig. 14).

To investigate the consequences, consider first the symmetric single tone excitation corresponding to Fig. 6 with $V_{\rm bo} = 0$ and $V_X = (1/2)V_o \cos(\omega t)$. In what follows, $V = 2V_X = V_{\rm ds}$.

Assuming that the $I(V)$ characteristic is such that the first three derivatives exist at $V = 0$

$$I_d = aV + bV^2 + cV^3 + o(V^3) \tag{21}$$

where a, b, and c are constants. For a symmetric model $b = 0$ therefore

$$I_d = I_1 \cos(\omega t) + I_3 \cos(3\omega t) + o\left(V_o^3\right) \tag{22}$$

where (cf. Fig. 15)

$$I_1 = aV_o + \frac{3}{4}cV_o^3 \tag{23}$$

$$I_3 = \frac{cV_o^3}{4}. \tag{24}$$

For asymmetric models, instead of (21), one has

$$I_d = \begin{cases} aV + bV^2 + cV^3 + o(V^3), & V \geq 0 \\ aV + b'V^2 + c'V^3 + o(V^3), & V < 0. \end{cases} \tag{25}$$

Here, as in [12] and [18], the first derivative exists and is continuous

$$a = I'(0) \tag{26}$$

$$b = \frac{1}{2} \lim_{V \downarrow 0} I''(V) = \frac{1}{2} I''(0+) \tag{27}$$

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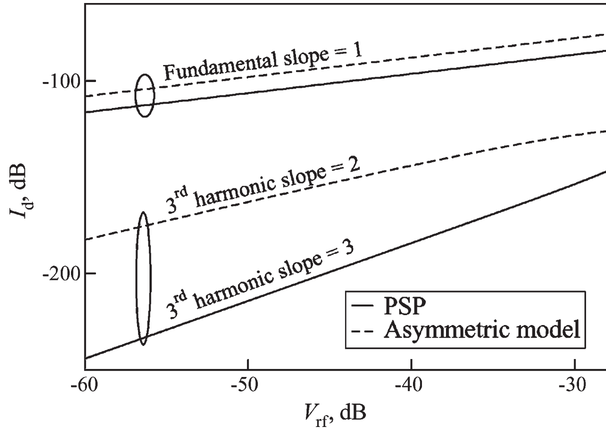

Fig. 15. Harmonic balance simulation results for symmetric excitations; $V_g = 0.4$ V, $W/L = 10/0.35$ μm, and fundamental frequency is 100 MHz. Default parameters are used for PSP.

$$b' = \frac{1}{2}\lim_{V\uparrow 0} I''(V) = \frac{1}{2}I''(0-) \tag{28}$$

$$c = \frac{1}{6}\lim_{V\downarrow 0} I'''(V) = \frac{1}{6}I'''(0+) \tag{29}$$

$$c' = \frac{1}{6}\lim_{V\uparrow 0} I'''(V) = \frac{1}{6}I'''(0-). \tag{30}$$

By (19)

$$b' = -b \tag{31}$$

$$c' = c. \tag{32}$$

In [18], the condition (18) was not imposed, and $c = c' = 0$. Note also that, in engineering practice, it is common to describe the case shown in Fig. 14 as "discontinuity of the second derivative" [18]. However, of course, according to the Darboux theorem, the derivative of the function cannot have discontinuity of the first kind; thus, we deal with the case where the second derivative of $I_d(V)$ does not exist at $V = 0$.[1] Using the symmetry condition (19) once more allows one to expand $I_d(V)$ in a Fourier series in the form (in our case $I_0 = I_2 = 0$)

$$I_d = \frac{I_0}{2} + \sum_{k=1}^{\infty} I_k \cos(k\omega t). \tag{33}$$

The amplitude of the third harmonic is

$$I_3 = \frac{4}{T}\int_0^{T/2} I(t)\cos(3\omega t)\,dt. \tag{34}$$

Simple computation yields

$$I_3 = \frac{4(b-b')V_o^2}{15\pi} + \frac{cV_o^3}{4} + o\left(V_o^3\right) \tag{35}$$

or, with reference to (31)

$$I_3 = \frac{8bV_o^2}{15\pi} + \frac{cV_o^3}{4} + o(V_o^3). \tag{36}$$

Here, the second term is the same as in (24), while the first one is associated with the singularity described by (25) and first studied in [18] for a special case. For small V_o, $I_3 \propto V_o^2$, which explains the slope of 2 dB/dB for the third harmonic observed in harmonic balance tests of some older models (see Fig. 15). Note also that (35) allows one to trace the gradual transition from the regime $I_3 \propto V_o^2$ to that of $I_3 \propto V_o^3$, as $|b - b'| = 2|b|$ is reduced relative to $|c|V_o$.

Returning to a standard asymmetric excitation version of the harmonic balance test shown in Fig. 10, one has (25) with $V = V_{\rm rf} = V_o\cos(\omega t)$ but without the symmetry condition $I_d(-V) = -I_d(V)$ and, hence, with $b' \neq -b$ and, in general, $c' \neq c$. This yields

$$I_3 = \frac{4(b-b')V_o^2}{15\pi} + \frac{(c+c')V_o^3}{8} + o\left(V_o^3\right). \tag{37}$$

Once again, the erroneous 2 dB/dB slope appears for the third harmonic, as illustrated in [10].

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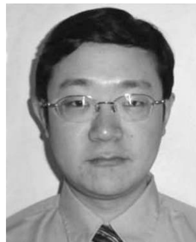

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