

Benchmarking the PSP Compact Model for MOS Transistors

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Abstract—Recently, the PSP model was selected as the first surface-potential-based industry standard compact MOSFET model. This work presents the results of several qualitative “benchmark” tests that over the last two years were used to verify the physical behavior of the new model and its usefulness for future generations of CMOS IC design. These include newly developed tests and previously unavailable experimental data stemming from low-power, RF, mixed-signal, and analog applications of MOSFETs.

I. INTRODUCTION

Compact MOSFET models are routinely required to satisfy the conflicting requirements of accurate reproduction of the minute details of transistor behavior (e.g. higher order transconductances) and computational efficiency. The latter inevitably implies the use of at least some empirical relations and various approximations in addition to the physics-based core of the model. By using the surface-potential-based approach to compact modeling [1], one can significantly increase the physics content of the compact model, but the use of semi-empirical relations cannot be completely eliminated. Hence it is necessary to prevent unphysical behavior of the compact models sometimes observed as an unintended consequence of various approximations [2]. Over the years two techniques were found to be particularly useful for assuring the high quality of compact models. The principle of the asymptotic correctness [3] essentially states that even empirical equations should become exact in extreme cases. This idea has been extensively used in the development and formulation of PSP. In addition, several “benchmark tests” have been formulated to address those aspects of the qualitative behavior of compact models that are of particular interest to circuit designers [4]–[6]. In this work, we demonstrate that the new industry standard PSP model satisfies the traditional tests [4]–[6], and we introduce several new tests that are brought about by the more stringent requirements imposed on new compact models by the continued scaling of MOS devices and their widespread RF applications.

II. TRADITIONAL BENCHMARK TESTS

Among the most important traditional benchmark tests are the slope-ratio (Fig. 1) and tree-top tests (Fig. 2), referring to the subthreshold behavior and G_m/I_d ratio, respectively [6]. The slope ratio is defined by

$$S_R = \frac{(I_2 + I_1)(V_{db2} - V_{db1})}{(I_2 - I_1)(V_{db2} + V_{db1})} \quad (1)$$

where in Fig. 1 $V_{db1} = 0.01V$ and $V_{db2} = 0.02V$. These tests essentially require the qualitative behavior of the model to be similar to that of the Sah-Pao [8] or charge-sheet model [9]. Since PSP is a direct descendant of these models, it easily passes both tests for all values of the model parameters. Another traditional test is the investigation of transcapacitances as functions of the terminal bias with fine resolution to detect possible singular behavior. Typical results shown in Fig. 3 indicate continuous and physical behavior of PSP transcapacitances, including the correct sign of C_{bd} and C_{gb} . The latter is problematic in some older models that separate charge and current submodels, but in PSP the symmetric linearization technique [1] allows one to achieve consistency of both submodels with the desired outcome illustrated in Fig. 3. The design of certain circuits, most importantly of passive RF mixers and transfer gates, requires symmetry of the model with respect to the source-drain interchange (the “Gummel Symmetry Test” or GST) [6], [7]. The circuit diagram for the GST is shown in Fig. 4 while typical results for PSP are presented as solid lines in Fig. 5, indicating that PSP passes this test. Three necessary conditions for this include a non-singular velocity saturation model [1], [7], an odd smoothing function describing the transition from the triode to saturation region of the MOSFET characteristics [1], [2], and the symmetry of the linearization procedure for the inversion and bulk charges as functions of the surface potential [1]. The above discussion refers exclusively to the qualitative behavior of the drain current and its derivatives for $V_{ds}=0$ (i.e. for $V_X=0$ in terms of the GST setup of Fig. 4). The results shown in Fig.

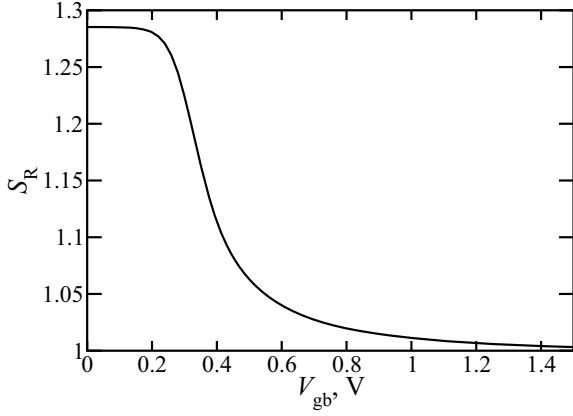


Fig. 1. Slope ratio test result for PSP with $W/L = 10/10\mu\text{m}$.

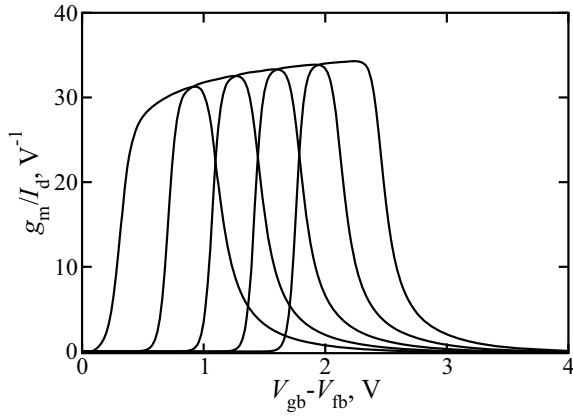


Fig. 2. Tree-top test results for PSP with $V_{ds} = 50\text{ mV}$, V_{bs} varies from -1 to 0.2V in 0.3V steps, $W/L = 10/10\mu\text{m}$.

5 demonstrate that with properly chosen parameters, the PSP model accurately reproduces the actual test data (symbols). Note that this is the first ever experimental investigation of the higher order derivatives for a MOS transistor operated at zero drain bias and that only one year ago it was impossible to model even the second derivative for $V_X=0$ with the industry standard MOSFET model.

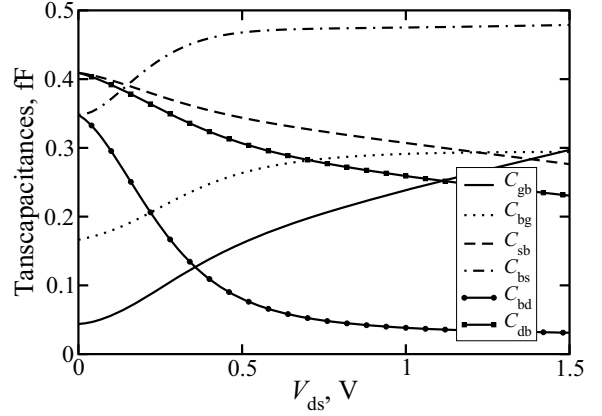
III. NEW TESTS

A. Subthreshold Region

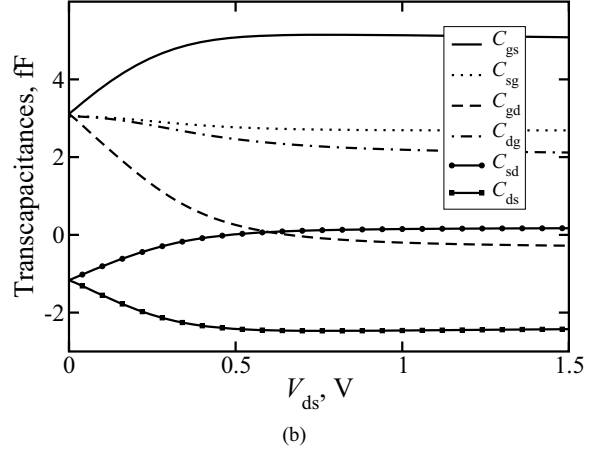
The subthreshold current can be expressed as [9]

$$I_d = \mu \frac{W}{L} C_{ox} \cdot \frac{\gamma \phi_t^2}{2\sqrt{\phi_{ss}}} e^{(\phi_{ss} - 2\phi_B - V_{sb})/\phi_t} (1 - e^{-V_{ds}/\phi_t}) \quad (2)$$

where μ is the mobility, C_{ox} is the oxide capacitance per unit channel region, γ is the body factor, ϕ_{ss} is the surface potential at the source end of the channel, ϕ_B is the ‘‘Fermi potential’’ and $\phi_t = k_B T/q$ is the ‘‘thermal potential.’’ The characteristic drain bias dependence $I_d \propto 1 - \exp(-qV_{ds}/kT)$ of the drain current in the subthreshold region can be conveniently



(a)



(b)

Fig. 3. Transcapacitances for PSP with $W/L = 10/0.08\mu\text{m}$.

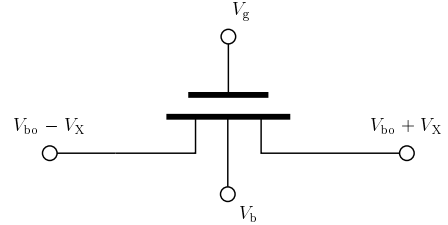


Fig. 4. Biasing scheme for the traditional Gummel symmetry test [6].

reformulated in terms of output conductance ($G_d = \partial I_d / \partial V_d$)

$$(\partial / \partial V_d) [G_d \cdot \exp(qV_{ds}/kT)] = 0 \quad (3)$$

implying zero slope on the $G_d \cdot \exp(qV_{ds}/kT)$ vs. V_{ds} plots. This is indeed observed in subthreshold, while increasing the gate bias leads to the formation of an inversion layer and, consequently, to a finite slope (cf. Fig. 6). There is an interesting connection of this characteristic behavior to the GST. It is common knowledge that when the charge-sheet model directly includes velocity saturation, the result is an unacceptable negative G_d in the saturation region. This problem is usually solved in compact models via the use of

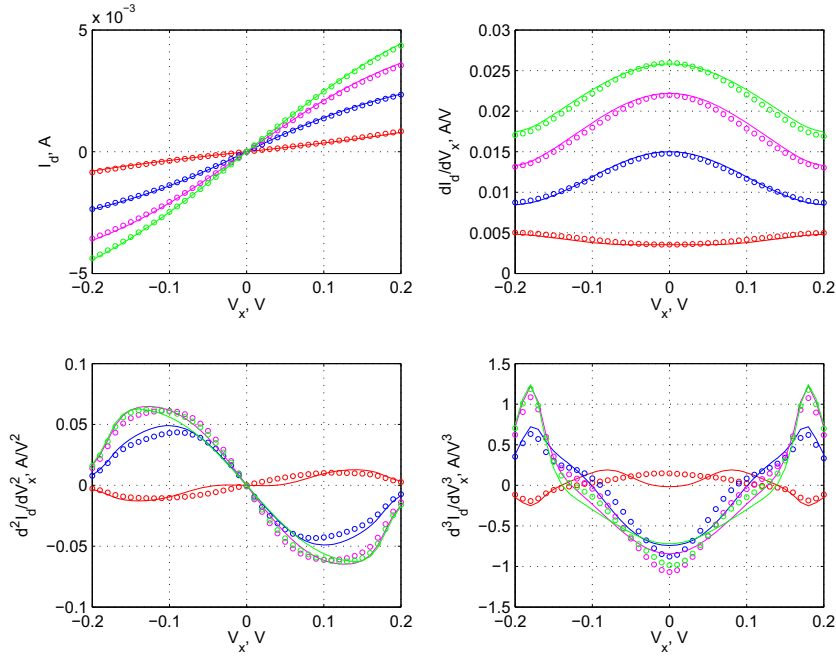


Fig. 5. Drain current and derivatives for Jazz Semiconductor $0.18\mu\text{m}$ technology, n-channel $10/0.18\mu\text{m}$ MOSFET; V_g varies from 0.6 to 1.8V in steps of 0.4V. Symbols represent experimental data while solid lines refer to PSP, V_x is defined in Fig. 4, $V_b = 0\text{V}$, $V_{bo} = 0\text{V}$.

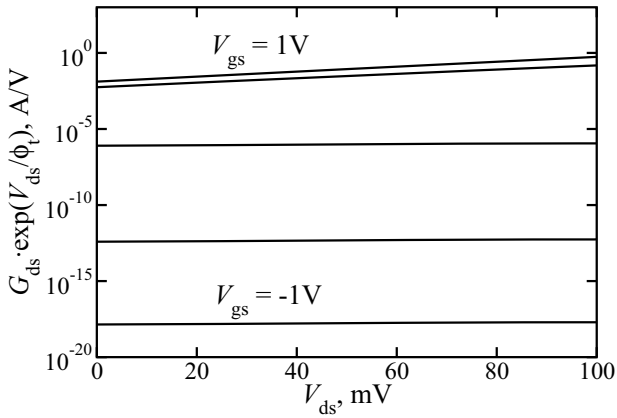


Fig. 6. PSP results for subthreshold region; V_{gs} varies from -1 to 1V in 0.5V steps.

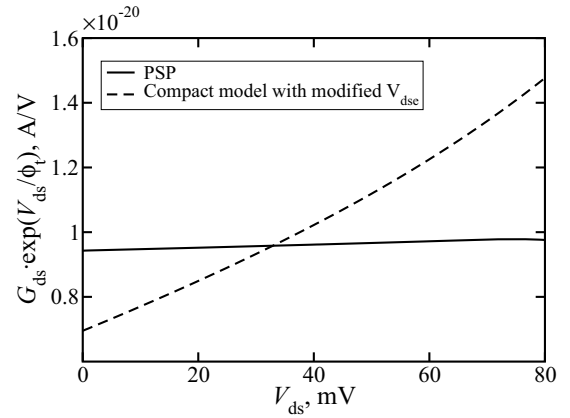


Fig. 7. Comparison of PSP and another compact model with modified V_{dse} for which dV_{dse}/dV_{ds} differs from 1 appreciably for $V_{ds} < 3\phi_t$; $V_{gs} = -1\text{V}$.

certain smoothing functions describing the transition from the triode to saturation regions by changing V_{ds} into the effective drain bias V_{dse} [1]. To pass the GST, the $V_{dse}(V_{ds})$ function has to be odd [3] with an additional requirement of unity slope for $V_{ds} = 0$ suggested in [10]. In fact, this condition is not required for passing the GST but is useful to ensure that (3) is satisfied. More precisely, one needs to require approximately unity slope of dV_{dse}/dV_{ds} for $V_{ds} < 3\phi_t$. If this condition is violated so is (3), as illustrated in Fig. 7.

B. Higher Order Derivatives in the Gummel Symmetry Test

To model the harmonic distortion in RF circuits operating with zero drain-source dc bias, it is now deemed necessary for compact models to be not just class $C^{(3)}$ (derivatives continuous to third order) but, at least, class $C^{(5)}$. The nature of the smoothing function

$$V_{dse} = \frac{V_{ds}}{\left[1 + \left(\frac{|V_{ds}|}{V_{dsat}}\right)^{\text{AX}}\right]^{\frac{1}{\text{AX}}}} \quad (4)$$

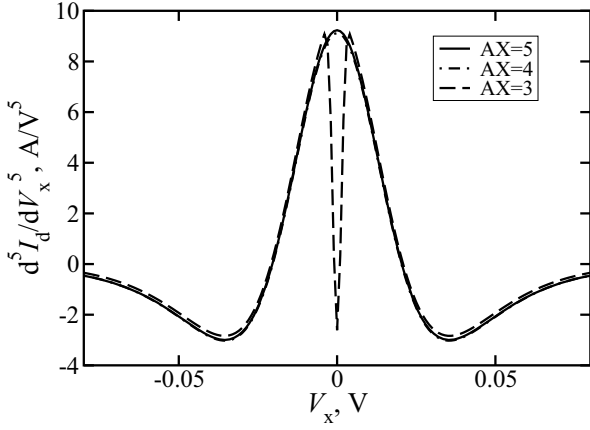


Fig. 8. 5th order derivatives for different \mathbf{AX} (cf. Fig. 4). For $\mathbf{AX} = 3$, condition (5) is violated.

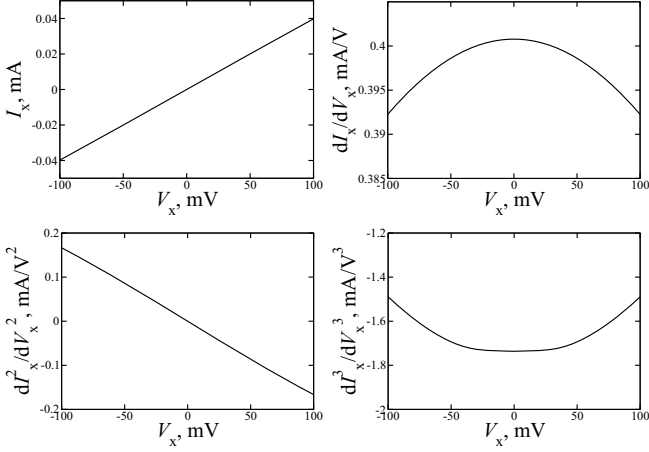


Fig. 9. Modified dc symmetry test for PSP, $I_X = (I_d - I_s)/2$, $V_g = 1\text{V}$, $V_b = -0.1\text{V}$, $V_{bo} = 0\text{V}$ with circuit diagram is still of Fig. 4.

used in PSP is such that class $C^{(3)}$ behavior is automatically guaranteed ($\mathbf{AX} > 2$), but in order for the n -th derivative to exist at $V_{ds} = 0$ it is necessary to impose the condition

$$\mathbf{AX} > n - 1 \quad (5)$$

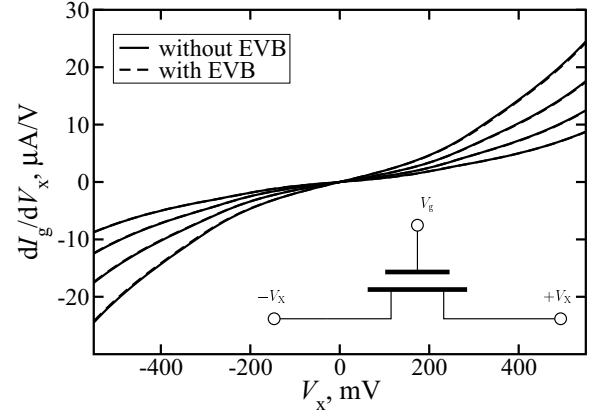
The local parameter \mathbf{AX} scales with the device effective channel length as

$$\frac{\mathbf{AXO}}{1 + \mathbf{AXL}/L} \quad (6)$$

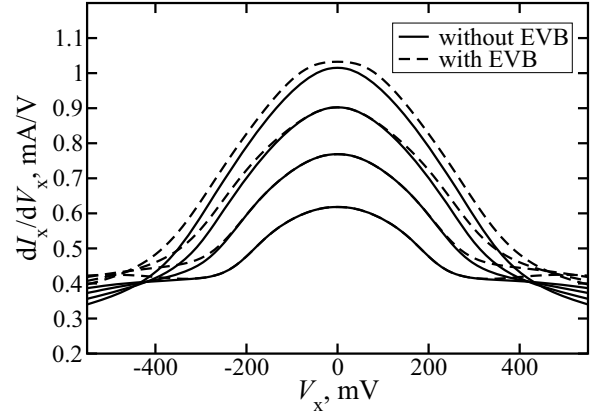
where \mathbf{AXL} is a global (scaling) parameter. For short-channel devices this limits the range of \mathbf{AXL} making it more difficult to fit the output conductance G_d as a function of the drain bias. Typical results for $n = 5$ for different values of \mathbf{AX} are shown in Fig. 8. This limitation is not specific to PSP and, in fact, in the previous standard model the second derivative does not exist for $V_{ds} = 0$ [10].

C. Modified Symmetry Test

The traditional Gummel symmetry test generally does not apply in the presence of gate and substrate currents. For this



(a) Gate Current



(b) Drain Current

Fig. 10. Modified Gummel symmetry test for SOI MOSFET. Inset in (a) shows the biasing with V_X . The model parameters used here are extracted from typical 90-nm PD/SOI technology data. V_g varies from 0.7 to 1.0V in 0.1V steps, $W/L = 2/1\mu\text{m}$.

reason, a new test has been developed in [11]. Typical results including gate current are shown in Fig. 9 indicating that PSP passes this test. Another example is shown in Fig. 10 for a floating-body SOI MOSFET when valence-band electron (EVB) tunneling current is included [12], indicating that PSP-SOI also passes this symmetry test.

In addition to the dc symmetry test, the modified symmetry test [11] also includes a transcapacitance check. Fig. 11 shows the biasing scheme for an ac symmetry test. The results are shown in Fig. 12 in which

$$\delta_{cg} = \frac{i_{g-}}{i_{g+}} = \frac{C_{gs} - C_{gd}}{C_{gs} + C_{gd}} \quad (7)$$

where $i_{g-} = \text{Im}(I_g)$ with anti-phase source and drain ac excitations and $i_{g+} = \text{Im}(I_g)$ with in-phase source and drain ac excitations. Similarly, the symmetry of the source and drain charges can be tested by realizing that

$$\delta_{csd} = \frac{(i_{s-} + i_{d-}) + (i_{s+} - i_{d+})}{(i_{s-} - i_{d-}) + (i_{s+} + i_{d+})} = \frac{C_{ss} - C_{dd}}{C_{ss} + C_{dd}} \quad (8)$$

should be an odd function of V_X . The plots clearly show that PSP passes the test while another popular model fails.

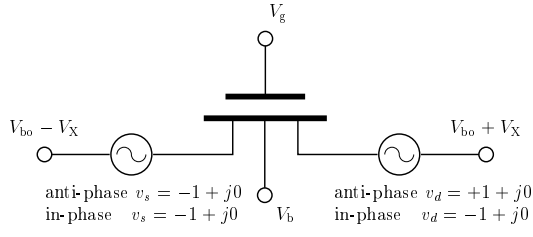


Fig. 11. Biasing scheme for modified ac symmetry test.

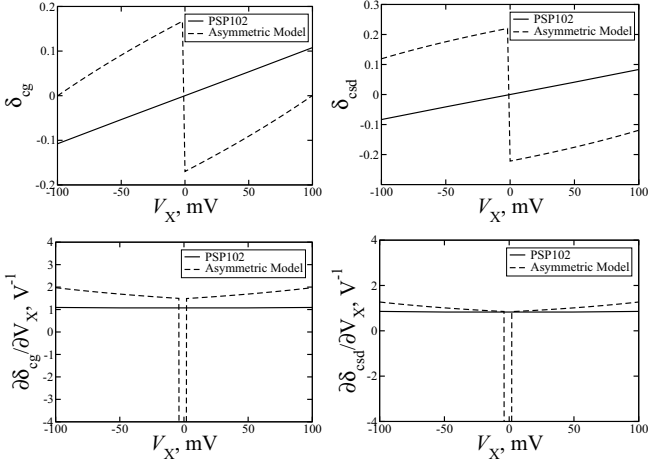


Fig. 12. Modified ac symmetry tests for PSP and another MOSFET model with $V_g = 1\text{V}$, $V_b = -0.1\text{V}$ and $V_{bo} = 0\text{V}$ (cf. Fig. 11).

D. Reciprocity

Generally speaking, MOSFET transcapacitances are non-reciprocal. However, for $V_{ds} = 0$ (a condition often useful for model parameter extraction), reciprocity is recovered. PSP is one of only two models (the other is MM11 [13]) in which the reciprocity condition is approximately satisfied for $V_{ds} = 0$ with accuracy sufficient for engineering applications (Fig. 13). The small deviation from reciprocity is associated with the charge-sheet approximation [13]. Note that the symmetry of the model assures that in PSP $C_{ds} = C_{sd}$ exactly for $V_{ds} = 0$ (Fig. 3(b)).

E. Back-bias clamping

Compact model formulation is often simplified by softly limiting the back bias V_{bs} at the 0.8V level. Since for $V_{bs} > 0.8\text{V}$ transistor currents are dominated by source and drain pn junctions, this clamping is inconsequential as long as it is done in a non-singular manner (so that circuit simulations with disabled pn junctions are not compromised). The smooth V_{bs} clamping used in PSP is illustrated in Fig. 14.

IV. NON-QUASI-STATIC (NQS) AND NOISE MODEL TESTS

Qualitative behavior checks are also performed for the PSP NQS model. Using transmission line analysis, one can readily show that, for a long channel at $V_{ds} = 0\text{V}$, the MOSFET

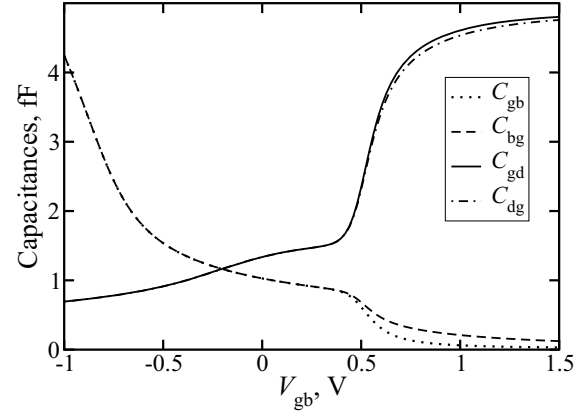


Fig. 13. Transcapacitances C_{gd} , C_{dg} , C_{gb} and C_{bg} for PSP with $W/L = 10/0.08\mu\text{m}$ at $V_{ds}=0$.

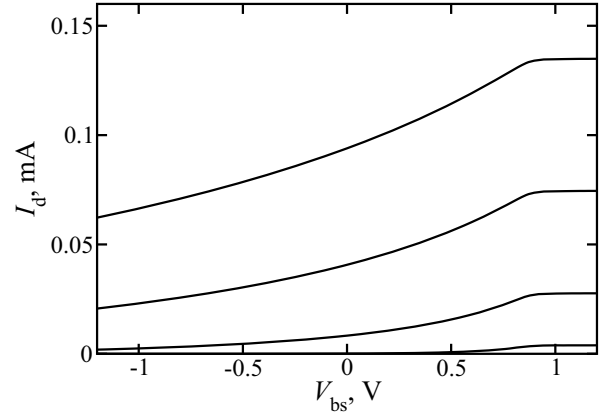


Fig. 14. Back-bias clamping of PSP for different gate biases; V_{gs} varies from 0.3 to 1.2V in 0.3V steps, $V_{ds}=1.2\text{V}$.

input impedance satisfies the relation [14]

$$R_{in} \equiv \lim_{f \rightarrow 0} \text{Re} \left(\frac{1}{y_{GG}} \right) = \frac{1}{12 \cdot g_{DS}} \quad (9)$$

A new test which follows from a similar transmission line analysis is developed. For a long channel device at $V_{ds} = 0\text{V}$, one should have

$$R_{DG} \equiv \lim_{f \rightarrow 0} \text{Re} \left(\frac{1}{y_{DG}} \right) = \frac{1}{6 \cdot g_{DS}} \cdot \left(1 + \frac{C_{dep}}{C_{ox}} \right) \quad (10)$$

Typical results for PSP shown in Fig. 15 indicate that both conditions are satisfied without any parameter adjustments.

In [15] the drain current noise model is tested using the so-called white-noise gamma factor γ , defined as $\gamma = S_{I_D} / (4k_B T g_{do})$, where g_{do} is the zero-drain-bias output conductance. For $V_{ds} = 0\text{V}$, the Nyquist law applies and $\gamma = 1$ should hold irrespective of the inversion condition. At elevated V_{ds} , γ should approach 1/2 in weak inversion (corresponding to “shot noise”), whereas in saturation it should approach the well-known value of 2/3. Indeed PSP complies with this new test, as demonstrated in Fig. 16.

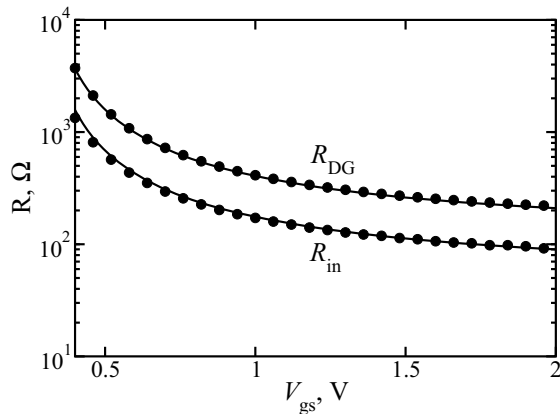


Fig. 15. R_{in} and R_{DG} as functions of gate-source bias. Symbols represent PSP simulations using a long-channel parameter set while lines refer to theoretical values of R_{in} and R_{DG} .

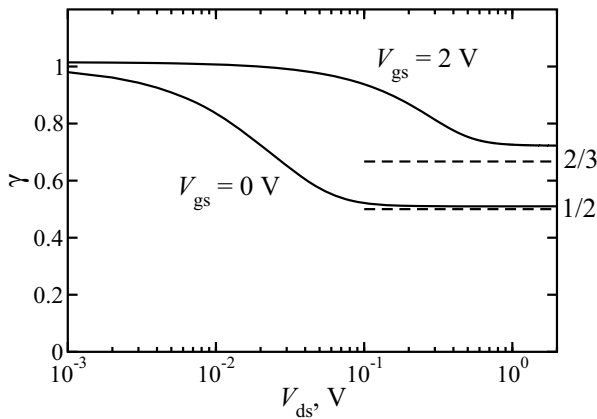


Fig. 16. White noise gamma factor as a function of drain-source voltage.

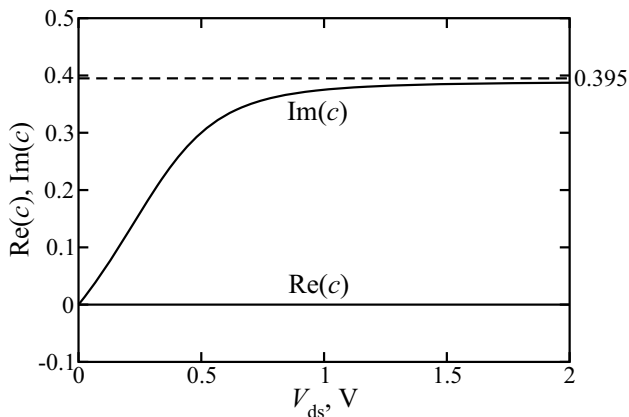


Fig. 17. Real and imaginary parts of correlation coefficient versus drain-source voltage.

The correlation coefficient between induced gate noise and drain current thermal noise for a long channel device in saturation should be $c = 0.395j$ [16]. One can show [15] by a

symmetry argument that c should be equal to zero at $V_{ds} = 0V$. Fig. 17 shows that the imaginary part of c increases from 0 at $V_{ds} = 0 V$ to approximately $0.395j$ in saturation.

V. CONCLUSION

A battery of traditional and newly developed benchmark tests is available to model developers to assure the correct qualitative behavior of compact MOSFET models. The application of these tests is illustrated using the new industry standard PSP model. Experimental data for higher-order derivatives of the drain current at $V_{ds} = 0$ are presented for the first time ever and are accurately reproduced by PSP.

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