PSP-Based Scalable MOS Varactor Model

J. Victory[1], Z. Zhu[2], Q. Zhou[2], W. Wu[2], G. Gildenblat[2], Z. Yan[1], J. Cordovez[1], C. McAndrew[3], F. Anderson[4], J. C. J. Paasschens[5] , R. van Langevelde[6], P. Kolev[7], R. Cherne[8], and C. Yao[9]

[1]Jazz Semiconductor, Newport Beach, CA, [2]Ira A. Fulton School of Engineering, Department of Electrical Engineering Arizona State University, Tempe, AZ, [3]Freescale Semiconductor, Tempe, AZ, [4]IBM, Burlington, VT
[5]NXP Semiconductors, Gerstweg 2, 6534 AE Nijmegen, The Netherlands, [6]Philips Research, Eindhoven, The Netherlands
[7]Formerly with RFMD, San Diego, CA, now with Qualcomm, San Diego, CA
[8]Intersil Corporation, Palm Bay, Florida, [9]Analog Devices, Inc., Wilmington, MA
E-mail: james.victory@jazzsemi.com

Abstract - **A physically based scalable model for MOS Varactors is presented. The model includes a PSP-based analytical surface potential charge formulation, MOS varactor specific gate current models, and physical geometry and process parameter based parasitic modeling. Key device performances of capacitance and quality factor Q are validated over voltage, frequency, and geometry, for several technologies. The model, implemented in Verilog-A, provides robust and accurate RF simulation of MOS varactors. A VCO design application is detailed.**

I. INTRODUCTION

Continuing advances in RF CMOS technology have made it a viable platform for RF/analog and millimeter wave circuits. Design of these circuits requires accurate, scalable compact models for the active transistors and passive components in a given technology. This includes MOS varactors, which provide frequency tuning for circuits such as voltage-controlled oscillators (VCOs). MOS varactors are typically the only tuning elements offered in RFCMOS process design kits.

In 2006, the Compact Model Council (CMC) launched a MOS varactor model standardization process, forming a subcommittee of modeling engineers from across the industry. The subcommittee defined requirements for an industry standard MOS varactor model, and improvements needed to the model of [1]. One requirement was consistency with the new industry standard PSP MOSFET model [2]. As the MOSFETs and MOS varactors in a given technology are closely related, consistency between models for related MOS devices is highly desirable. Characterization of technology parameters related to oxide thickness, quantum mechanical (QM) effects, poly depletion, and fringing capacitance for example can be done for one device type (e.g. a MOSFET) and then the parameters used for another device (e.g. a MOS varactor). Moreover, consistent MOS device models enable statistical model consistency and correlation across a technology model library.

Prior MOS varactor models are predominantly subcircuits that include a frequency independent intrinsic capacitance through either a MOSFET (BSIM) model or a polynomial behavioral equation. Device parasitic resistance, capacitance and inductance are included through lumped elements, and device performances are validated over a small geometry and frequency space [3]-[6].

This paper advances the state-of-the-art by providing a physically based scalable MOS varactor model, MOSVAR, consistent with the industry standard PSP MOSFET model. Parasitic components, responsible for the variable reactance of the device, are modeled physically. A gate current model, uniquely derived for the MOS varactor structure, is presented here for the first time. The model is implemented in the Verilog-A language.

Section II details MOS varactors and the MOSVAR model. Model validation over a wide range of technologies is presented in section III. Section IV investigates MOSVAR scaling effects on critical VCO performances such as the VCO gain KVCO and phase noise.

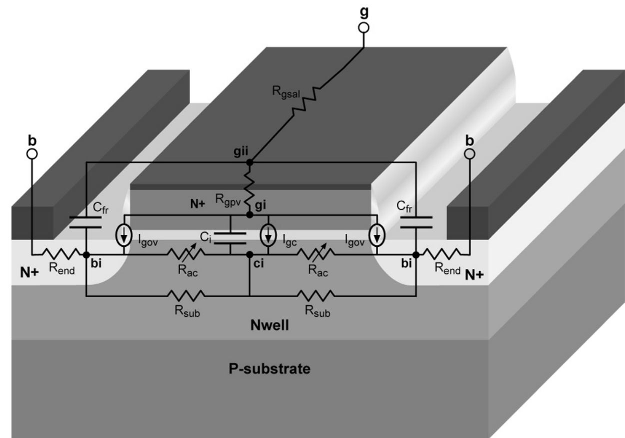

Fig. 1 N+ poly/Nwell MOS varactor with MOSVAR model network

II. DEVICE AND MODEL DESCRIPTION

Fig. 1 shows a typical N+ poly/Nwell MOS varactor with the MOSVAR model equivalent network embedded in the physical layout. The model includes elements related to the poly-silicon gate, the oxide, and the well or bulk region below the oxide, including contacts to the well. MOSVAR includes neither the parasitics associated with the well and underlying substrate (P-substrate here), nor the metal parasitics shown in

Fig. 2. As varactors can be formed in multiple well configurations and devices can be arrayed and connected through various metallization schemes, layout and substrate parasitics are better handled at a subcircuit level. For this reason, MOSVAR is a 3-terminal model with the terminals *g, b,* and *bi*. The *bi* terminal allows for connection of the Nwell-P-substrate parasitic network. (Note that from symmetry only one half of the networks in Fig. 1 and Fig. 2 is actually included in the MOSVAR model; the mirrored networks are included for mapping to the physical structure.)

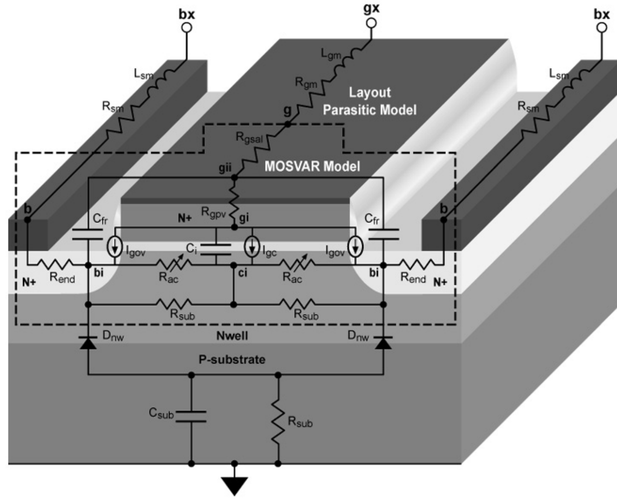

Fig. 2 N+ poly/ Nwell MOS Varactor with MOSVAR model and layout/substrate parasitics embedded

Differential varactors, formed in a common well with alternating gates forming the differential terminals, are common in differential VCO design [6], [7]. The MOSVAR model is easily extended to differential designs by making the *gi* or *gii* terminal external, to allow differential connection of the parasitic gate-to-gate capacitance.

Table 1 lists the MOSVAR model parameters; those common to PSP are in shaded boxes. The changes in components C_i, C_{fr}, R_{ac}, R_{sub}, R_{end}, and R_{gsal}, originally presented in [1], are reviewed here. Element multiplicity is scaled through M. The model includes extensive temperature modeling where temperature related parameters begin with "ST" in Table 1. Details of the temperature modeling and verification are not presented here for brevity.

Parameter	Description
TOXO	Oxide thickness
VFBO	Flatband voltage
NSUBO	Substrate (Well) doping level
NPO	Polysilicon doping level
QMC	Quantum mechanical correction factor
DLQ	Length delta for intrinsic capacitance
DWQ	Width delta for intrinsic capacitance
DWR	Width delta for substrate resistance
NGCON	Number of gate contacts (1 or 2)
TAU	Time constant for inversion charge recombination/generation
CFRL	Fringing capacitance in length direction
CFRW	Fringing capacitance in width direction
RSHG	Gate sheet resistance
RPV	Vertical poly contact resistance
REND	End resistance/unit width
RSHS	Substrate (Well) sheet resistance
UAC	Accumulation layer zero bias mobility
UACRED	Accumulation layer mobility reduction factor
STVFB	Temperature exponent of VFB
STRSHG	Temperature exponent of RSHG
STRPV	Temperature exponent of RPV
STREND	Temperature exponent of REND
STRSHS	Temperature exponent of VFB
STUAC	Temperature exponent of UAC
NOVO	Doping of overlap region
LOV	Length of overlap region
GCOO*	Gate tunneling energy adjustment
IGINVLW*	Gate channel current pre-factor
IGOVW*	Gate overlap current pre-factor
STIG*	Temperature coefficient for iginv and igov
GC2O*	Gate current slope factor
GC3O*	Gate current curvature factor
CHIBO*	Tunneling barrier height

Table 1. MOSVAR Parameters , parameters common to PSP are shaded gray, *Separate values of parameters are used for each component of gate tunneling current

A. Frequency Dependent Intrinsic Capacitance C_i

MOSFET models assume a frequency independent inversion charge, supplied from the source and drain. Without source or drain regions the inversion charge in an accumulation-mode MOS varactor depends on frequency, since it is thermally generated. In MOSVAR, the intrinsic charge is modeled through a frequency dependent analytical surface potential model fully consistent with the PSP surface potential model [1], [8]. The MOSVAR QM model is from PSP. However, accumulation in the poly-silicon, ignored in PSP, is included in MOSVAR.

B. Fringing Capacitance C_{fr}

Overlap and fringing capacitances are lumped together into C_{fr}. Parasitic capacitances along the gate width and length are included. The length component is generally neglected in practice since the poly edge termination along the lengths is over field or shallow trench oxide and the length is small compared to the width. The total fringe capacitance is

$$(1) \qquad C_{fr} = 2 \cdot \left(\mathrm{CFRW} \cdot W_g + \mathrm{CFRL} \cdot L_g \right) \cdot M$$

C. Well and Accumulation Resistance R_{ac}, R_{sub}, and R_{end}

The well or bulk under the gate oxide forms a parallel combination of a bias independent well resistance and a bias dependent accumulation resistance. The assumption of bias independence of the well resistance in depletion follows from the high doping of the surface regions in sub-micron MOSFET

technologies; variation of the thin depletion region under the oxide has a negligible effect on the resistance of the well. Measurements validate this assumption; they show no appreciable well resistance variation with gate bias. The bias independent well resistance is

$$R_{sub} = \mathrm{RSHS} \cdot \frac{L_g}{(12 \cdot W_g \cdot M)} \quad (2)$$

As the gate bias increases above the flatband voltage, an accumulation layer forms, therefore

$$R_{ac} = \frac{L_g}{(W_g \cdot \mu ac_V \cdot Q_{ac} \cdot M)} \quad (3)$$

where $\mu ac_V = \mathrm{UAC}/[(1+\mathrm{UACRED}\cdot(\mathrm{VFBO}-V_{GBi}))]$ including low-field surface mobility and mobility degradation parameters, and Q_{ac} is the accumulation charge density determined directly from the surface potential.

A significant portion of the MOS varactor resistance is from the well end resistance, formed by the lightly doped source/drain contact regions, the salicided contact diffusion, and the contact resistance. This resistance does not change with gate length and is the factor that limits the maximum Q for minimum L_g. The end resistance is given by

$$R_{end} = \frac{\mathrm{REND}}{(2 \cdot W_g \cdot M)} \quad (4)$$

where the factor 2 accounts for the symmetry of the gate segment.

D. Poly Gate Resistance R_{gsal} and R_{gpv}

The salicided poly gate resistance is given by the well known expression

$$R_{gp} = \mathrm{RSHG} \cdot \frac{W_g}{(3 \cdot L_g \cdot \mathrm{NGCON}^2 \cdot M)} \quad (5)$$

The silicide to poly contact resistance as described by Litwin [9] and implemented into a MOSFET gate resistance model by Scholten *et al*. [10], is given by

$$R_{gpv} = \frac{\mathrm{RPV}}{(W_g \cdot L_g \cdot M)}. \quad (6)$$

The two gate resistance components enable accurate, scalable modeling of total gate resistance. Additionally, the *gii* node allows for physical placement of the fringing capacitance C_{fr}, directly affecting the quality factor.

D. Gate Current

Engineering models of the tunneling current in MOSFETs have been discussed in [11], [12] and [13]. The tunneling current model in MOS varactors is conceptually similar, but differs in several significant aspects. First, there are different possible polarities of gate and silicon dopants, leading to different possible tunneling current components, such as electron conduction band (ECB), electron valence band (EVB) and hole valence band (HVB), see Fig. 3. A detailed physical analysis is presented in [14]. It is clear that HVB tunneling, which is not essential in bulk MOSFETs, may become significant for varactors. Second, the surface potential in varactors is position-independent, which simplifies the tunneling current model. Both channel and overlap tunneling current densities are computed using Tsu-Esaki formula [15]

$$J_g = \frac{q \cdot m_{ox}^* \cdot k_B T}{2\pi^2 \cdot \hbar^3} \int D(E_x) F_s(E_x) dE_x \quad (7)$$

where $D(E_x)$ is the transmission coefficient, $F_s(E_x)$ is the supply function, E_x is kinetic energy associated with motion in the direction normal to the potential barrier and m_{ox}^* is the effective electron mass in oxide. For the purpose of compact modeling, we use the mono-energetic approximation of the integral in (7), as developed in [12], [13] and used in the PSP model [16]. In the mono-energetic approximation $E_x = V_{ox}$ for $V_{ox} > 0$ and $E_x = 0$ for $V_{ox} < 0$, with a smoothing function used to provide non-singular behavior at $V_{ox} = 0$.

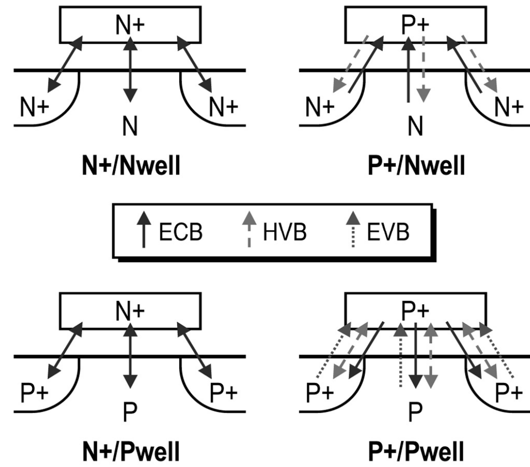

Fig. 3 Dominant tunneling current components in different MOS varactor structures

The resulting expressions for the different tunneling current components differ primarily in the supply function. For example, in case of the N^+/NWELL structure shown in Fig. 1, the HVB current density is

$$J_{g,HVB} \approx J_{g0,HVB} \cdot D_{HVB} \cdot F_{s,HVB} \quad (8)$$

where $J_{g0,ECB}$ is a model variable, theoretically equal to $qm_{ox}^*(k_B T)^2/(2\pi^2 \cdot \hbar^3)$, and the transmission coefficient is estimated using the WKB method as

$$D_{HVB} = \exp\left[-B_{HVB}\left(\frac{3}{2} - \mathrm{GC2O}\cdot z_g - \mathrm{GC3O}\cdot z_g^2\right)\right] \quad (9)$$

.

Here $B_{HVB} = 4t_{ox}\sqrt{2m_{ox}^{*} \cdot \text{CHIBO}}/3\hbar$ where for HVB tunneling, CHIBO is the band offset between the valence bands of Si and that of SiO_2 and $z_g = V_{ox}/\text{CHIBO}$ where V_{ox} denotes oxide voltage. The model parameters GC2O and GC3O compensate for the use of the WKB approximation and for uncertainty in m_{ox}^{*}. The surface potential based HVB supply function is

$$F_{s,HVB} = \ln\left[\frac{1+\Delta_{HVB}\cdot\exp(V_{gb}/\phi_t)}{1+\Delta_{HVB}}\right] \quad (10)$$

where $\Delta_{HVB} = \exp[-(\psi_s + E_g/q - \alpha_b + E_x/q)/\phi_t]$. Here ψ_s denotes surface potential, E_g is the silicon bandgap, $\alpha_b = (E_c - E_F)/q$ in the bulk and V_{gb} is the gate bias referenced to body-diffusion bias which is almost always grounded to suppress substrate noise.

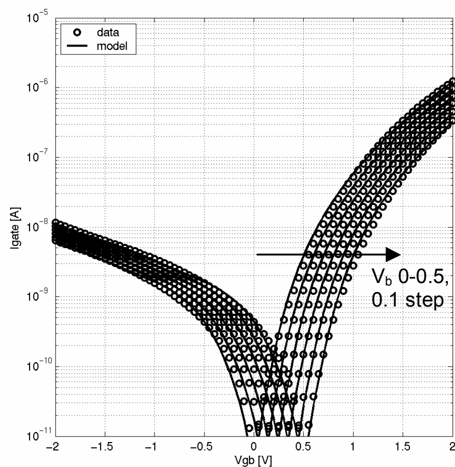

Fig. 4 Igate over bias for 1.2V N+/Nwell MOS Varactor, W_g=3µm, L_g=0.5µm

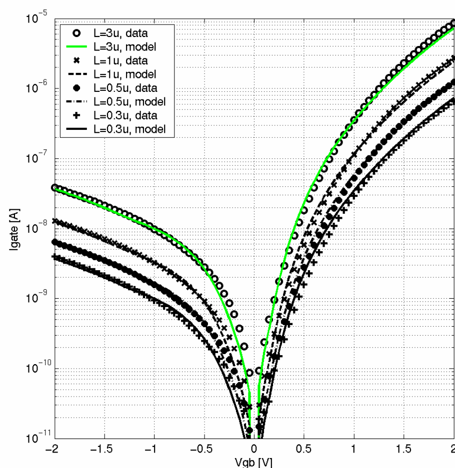

Fig. 5 Igate over L_g for 1.2V N+/Nwell MOS Varactor, W_g=3µm, V_b=0

The remaining components of the tunneling current are evaluated similarly. Typical results for N+/NWELL structure are shown in Fig. 4 and Fig. 5. Nine devices with different length and width were fitted simultaneously using the same parameter set, with no scaling parameters for the gate current.

III. Silicon Validation of RF Model

Robust measurement and extraction procedures for predominantly process and geometry based parameters across a wide geometry, bias, and frequency space for 0.18 µm RFCMOS technology were presented in [1]. The techniques are further validated in this work on data from the Jazz 0.13 µm RFCMOS technology. At low frequencies (500MHz), the total gate capacitance is $\text{Im}(y_{11})/(2\pi f)$. $Q=\text{Im}(y_{11})/\text{Re}(y_{11})$ values are extracted in the GHz range where $\text{Re}(y_{11})$ is within the dynamic range of the network analyzer (NWA).

Fig. 6 through Fig. 8 show C(V), Q(V), and Q(f) respectively, for an N+/Nwell 1.2V oxide device with varying L_g. The model accurately predicts the reduced tuning range (C_{max}/C_{min}) with decreasing L_g due to the influence of C_{fr}. Further, the significant decrease in Q with increasing L_g due to increasing well resistance is modelled well. Fig. 9 through Fig. 11 show the same quantities for varying W_g. The model accurately predicts the decrease in Q with increasing W_g due to increased R_{gsal}. The mismatch between model and data for Quality Factors above 125 is attributed to dynamic range limitations of the NWA. Fig. 12 and Fig. 13 show the accuracy of simulation of C(V) and Q(V) for N+/Nwell 3.3V oxide devices with varying L_g. The thicker oxide gives a lower tuning range for the 3.3V MOS varactors. Combined with the 1.8V N+/Nwell data presented in [1], the MOSVAR model is thus shown to be valid for wide range of devices with varying oxide thicknesses (1.9-7.0 nm).

Fig. 14 shows C(V) for 1.8V N+/Nwell and P+/Nwell varactors from Jazz's 0.18µm RFCMOS technology. The P+/Nwell MOS varactor is of particular interest since the C(V) tuning is shifted to the positive V_{gb} range, facilitating simpler VCO topologies like those used for junction varactors. In addition, the P+ poly does not deplete in the accumulation region, increasing the tuning range compared to the N+ poly device. The model predicts the one bandgap shift in flatband voltage in changing from N+ to P+ poly.

IV. VCO Performance

Modern day RF standards, such as WLAN, WiMAX, UWB, automotive radar and high speed optical communications systems use high frequency VCOs for frequency synthesis and system timing [17], [18], [19]. In order to obtain a high-frequency oscillator with high frequency-accuracy, high-frequency VCO's are embedded in frequency synthesizers which use a high-precision (low-frequency) oscillator as input. In a typical VCO, a tank circuit, consisting of an integrated inductor and a MOS varactor, controls the oscillation frequency.

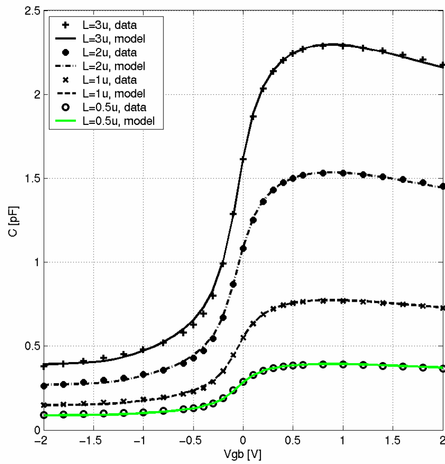

Fig. 6 C(V) for 1.2V N+/Nwell MOS Varactors, varying L_g

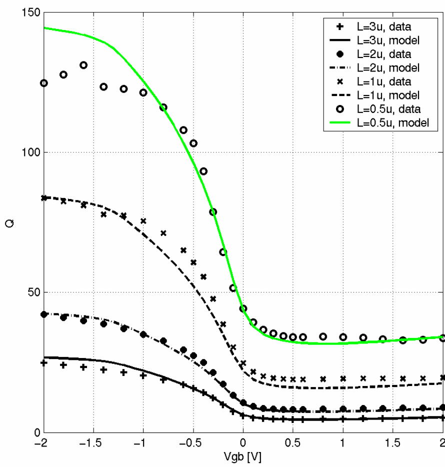

Fig. 7 Q(V), 4GHz for 1.2V N+/Nwell MOS Varactors, varying L_g

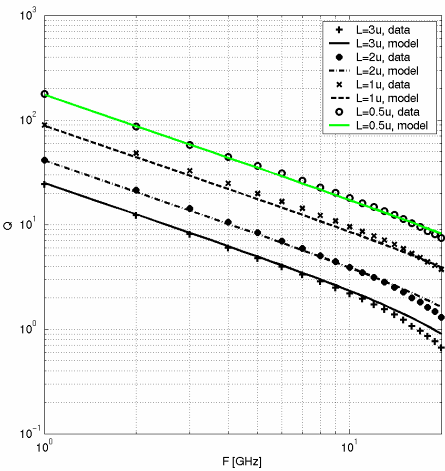

Fig. 8 Q(f), V_{gb}=0 for 1.2V N+/Nwell MOS Varactors, varying L_g

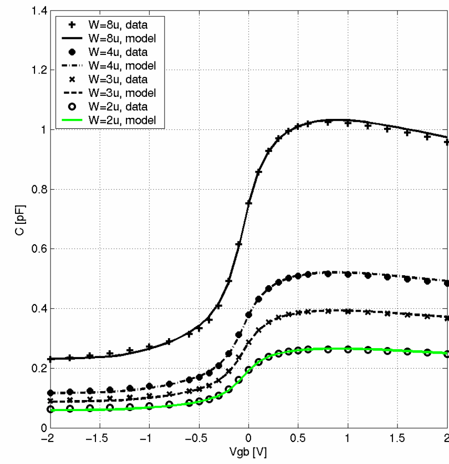

Fig. 9 C(V) for 1.2V N+/Nwell MOS Varactors, varying W_g

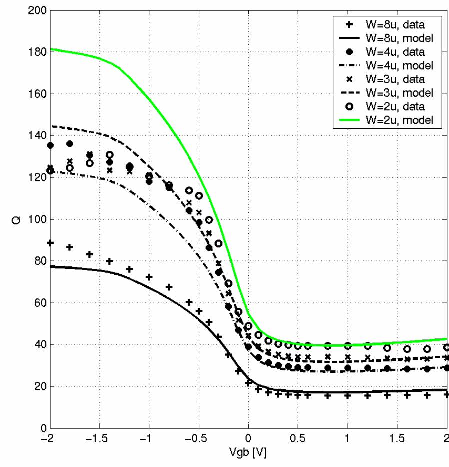

Fig. 10 Q(V), 4GHz for 1.2V N+/Nwell MOS Varactors, varying W_g

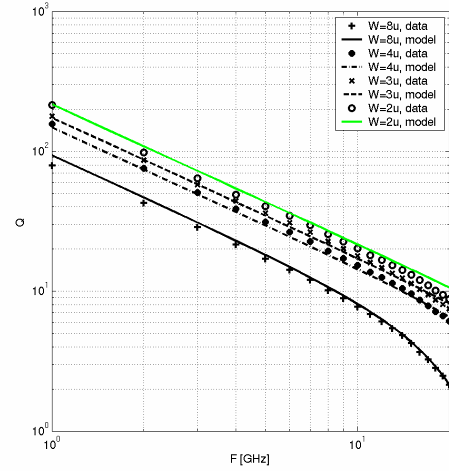

Fig. 11 Q(f), V_{gb}=0 for 1.2V N+/Nwell MOS Varactors, varying W_g

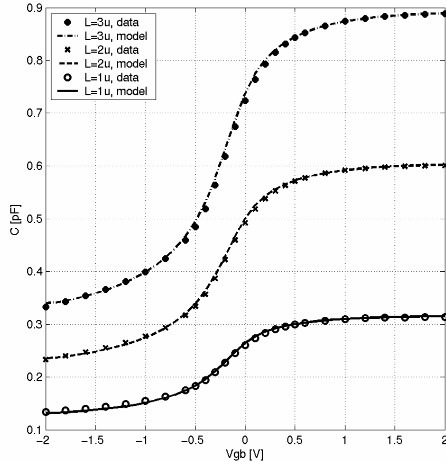

Fig. 12 C(V) for 3.3V N+/Nwell MOS Varactors, varying L_g

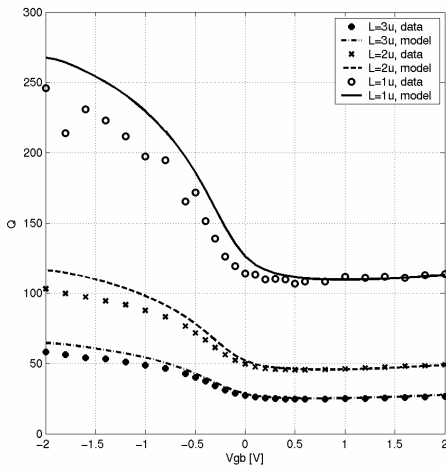

Fig. 13 Q(V) , 2 GHz for 3.3V N+/Nwell MOS Varactors, varying L_g

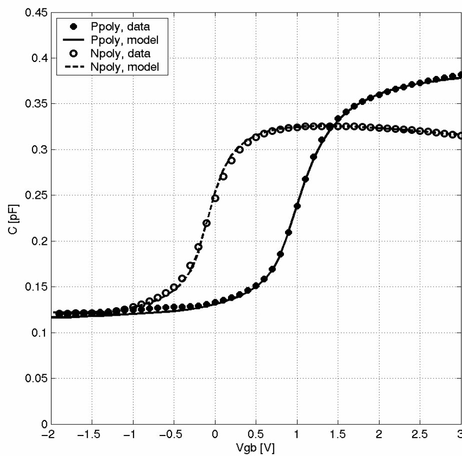

Fig. 14 C(V) for 1.8V N+/Nwell and P+/Nwell MOS Varactors, W_g=3μm, L_g=0.5μm

Fig. 15 shows an RF CMOS VCO, based on the negative resistance principle, using complementary cross coupled NFET and PFET pairs. This topology of voltage limited oscillator offers a larger available transconductance, decreased switching times, and tighter output symmetry than a standard NFET-only topology [20]. This gives improved phase noise (*PN*) and simplifies design. The VCO oscillation frequency is set by the differential inductor (L) and MOS varactor (C1 and C2) tank. Resistive tank losses are compensated by the negative resistance of the cross coupled pairs, enabling sustained oscillation.

The tank quality factor (Q_{tank}), which directly affects the phase noise of the VCO, is

$$Q_{tank} = \frac{Q_L \cdot Q_C}{Q_L + Q_C} = \frac{\omega L}{R_L + \omega^2 LCR_C}, \tag{11}$$

derived using the approximations for the tank components:

$$Q_L = \omega L / R_L \quad , \quad Q_C = 1/\omega CR_C \ . \tag{12}$$

R_X (where X denotes L or C) is the resistive loss for each component in the series tank path. Eq. (11) shows that as frequency increases, Q_{tank} approaches Q_C. Fig. 16 shows Q for three inductors designed to peak at 2, 5, and 10GHz, respectively. The inductor Q deviates from the ideal Q_L at high frequencies, peaking and decreasing due to skin effect and capacitive losses. The inductance is decreased by lowering the conductor length, which reduces capacitive losses. This in turn extends the range of ideal Q_L behavior with frequency, giving a higher peak Q for higher frequency applications. Varactors scaled through parallel multiplicity of fixed $W_g \times L_g$ devices, where $C \cdot R_C$ is constant, show a steady decrease in Q with frequency as shown in Fig. 16. At 2GHz, Q_L is roughly an order of magnitude lower than Q_C and hence dominates Q_{tank}. At 5GHz and above, Q_C is of the same order or lower than Q_L, clearly affecting Q_{tank}.

Leeson's phase noise model [20] provides additional insight into the varactor impact on phase noise. It relates the phase noise transfer function $H(j\Delta\omega)$ to the oscillator parameters by

$$|H(j\Delta\omega)|^2 = \frac{1}{4(Q_{tank})^2} \left(\frac{\omega_0}{\Delta\omega} \right)^2 \tag{13}$$

where ω_0 is the oscillator center frequency and $\Delta\omega$ is the offset frequency from ω_0 where the phase noise measurement is taken. At frequencies where Q_C dominates, (11) and (13) show that $|H(j\Delta\omega)|^2 \propto (R_C)^2$. Fig. 17 shows *PN* simulations of the VCO with the MOSVAR model. The *PN* increases with L_g, as expected due to the increased R_C. In addition, dPN/dLg increases at higher frequencies due to the increased influence of Q_C compared to Q_L..

In addition to PN, VCO tuning dynamics are commonly benchmarked through the VCO gain, KVCO, defined as

$$KVCO = \left|\frac{d\omega}{dV}\right|. \quad (14)$$

For the case of the LC circuit, $\omega = 1/\sqrt{LC}$. The voltage controlled varactor capacitance is given by

$$C = C_i' \cdot W_g \cdot L_g + 2 \cdot \mathrm{CFRW} \cdot W_g \quad (15)$$

where C_i' is the intrinsic MOS capacitance per unit gate area and the fringing capacitance in the length direction (CFRL) is assumed to be negligible. The derivative of C with respect to voltage is

$$\frac{dC}{dV} = \frac{dC_i'}{dV} \cdot W_g \cdot L_g . \quad (16)$$

Given $\omega = 1/\sqrt{LC}$, combining (14) and (16) yields

$$KVCO = \frac{\omega}{2} \cdot \frac{L_g}{C_i' \cdot L_g + \mathrm{CFRW}} \cdot \frac{dC_i'}{dV} \quad (17)$$

which for small L_g approaches

$$KVCO = \frac{\omega}{2} \cdot \frac{L_g}{\mathrm{CFRW}} \cdot \frac{dC_i'}{dV} \quad (18)$$

and for the large L_g saturates to

$$KVCO = \frac{\omega}{2 \cdot C_i'} \cdot \frac{dC_i'}{dV} \quad (19)$$

Equations (18) and (19) provide direct insight into the behavior of KVCO over varactor length. Simulations of the KVCO vs. L_g, shown in Fig. 18, verify the physical accuracy of the MOSVAR model, facilitating evaluation of critical VCO design tradeoffs. For the first time, to the knowledge of the authors, this aspect of MOS varactor modeling is reported.

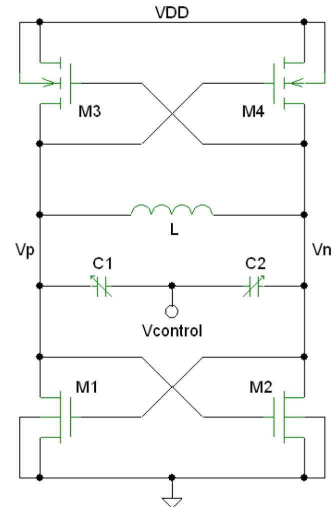

Fig. 15 VCO based on cross coupled NFET and PFET pairs

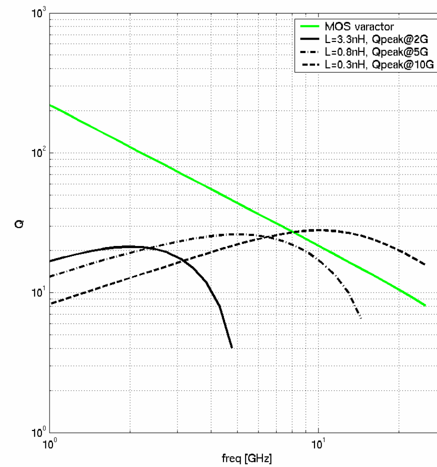

Fig. 16 Inductor and MOS varactor Q over frequency

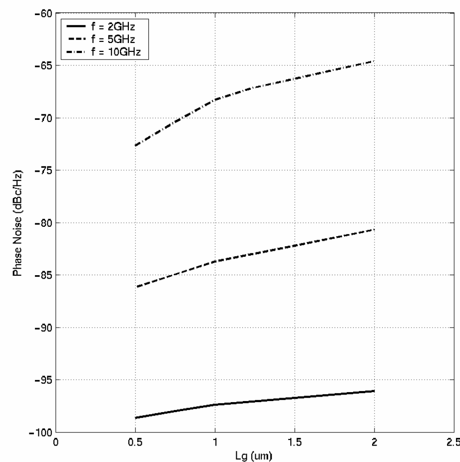

Fig. 17 Simulated phase noise at Δf=100KHz over L_g

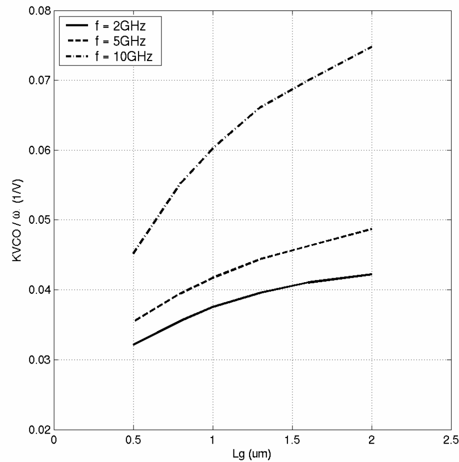

Fig. 18 Simulated KVCO over frequency and L_g

V. CONCLUSION

A complete surface potential-based MOS varactor model, consistent with the PSP MOSFET model, has been developed for RFCMOS and BiCMOS technologies. Reformulation and extension of the tunneling current models include MOS varactor specific ECB, EVB, and HVB components and contributions from both the channel and overlap regions. The model has been extensively verified by comparison with experimental C(V), Q(V,f), and gate leakage current data. The model contains physical process parameters, enabling simulation of changes in device characteristics associated with the changes in fabrication process. The scalability of the model enables simulation of critical trade-offs in VCO design.

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