DEVELOPMENT OF AN N-TYPE DEMOS ON A 0.6-μM PLATFORM FOR 18V ANALOG & DIGITAL APLICATIONS

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ABSTRACT

Anomalous hot-carrier induced on-resistance (Ron) and drive current degradations were observed in 18V n-type Drain Extended MOS (DEMOS) devices with various n-type Drain Drift (NDD) implant dosages. Under the same stress conditions, the device with higher NDD dosage while showing a higher substrate current (Isub) results in lower Idsat and ON-resistance (Ron) degradations. Optimal conditions for NDD implant which shift the high electric field peak causing away from the surface were introduced using technology computer aided design (TCAD) simulations. Consequently hot carrier induced degradation was suppressed as was verified by silicon measurements.

Index Terms—Drain-Extended MOS (DEMOS), n-type drain-drift (NDD), hot-carrier (HC), ON-resistance (Ron), TCAD

1. INTRODUCTION

The incorporation of a medium voltage (10-30V) transistor within a standard CMOS platform is required for medium-voltage analog and digital applications such as analog channel switching and LCD drivers and Boost Buck converters. Both lateral double diffused MOS (LDMOS) and drain-extended MOS (DEMOS) transistors can be easily incorporated in standard CMOS process. However, sometime DEMOS is more attractive because of its symmetrical drain/source structure. Due to the high drain operation voltages (Vds), hot carrier (HC) induced effects such as the degradation of on-resistance (Ron) and drive current and the value of the snapback (SB) voltage should be addressed.

This paper describes the development of a symmetrical n-type DEMOS on a standard 0.6μm platform for 18V applications. Three levels of n-type drain-drift (NDD) implant doses, low medium and high, are studied. Under a drain voltage stress, high Idsat and Ron degradations are observed for the low NDD dose, while its threshold voltage is not affected. This is an indication that the hot-electron induced degradation does not occur within the channel but in the NDD region. Increasing the NDD dose, while increasing the electric field and hence the hot carrier generation, results in a reduction of the SB voltage but showing lower hot carrier induced degradation [1] [2].

Technology computer-aided design (TCAD) simulations verified the existence of electric fields strengths higher than threshold for impact ionization in the NDD region in proximity to the gate edge. Based on TCAD simulation results a reliable n-DEMOS device with acceptable hot carrier induced degradation and high SB voltage was developed using an optimized NDD conditions.

2. MAIN PROCESS STEPS AND BASIC ARCHITECTURE

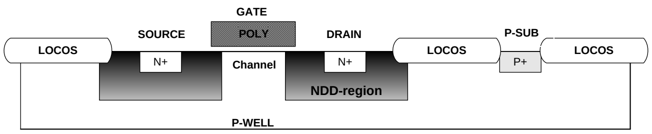


Figure 1 - Symmetrical n-type DEMOS architecture

The incorporation of 18V DEMOS devices in the standard 0.6µm CMOS process requires only minor adaptations. The cross-section of the n-DEMOS is depicted in Figure 1. Self-aligned NDD implant is followed by high temperature thermal drive-in process. The N+ source/drain, implanted after the poly sidewall oxide, is formed through a dedicated mask so as to enable minimization of the device Ron and its pitch without affecting the HC induced mechanisms. Study of three NDD dose values are presented here, low medium and high implanted perpendicularly with medium energy level. The NDD implant conditions are finally optimized using higher energy level and larger tilt angle.

3. EXPERIMENTAL DATA AND TCAD SIMULATIONS

The development of 18V n-DEMOS required extensive drain-engineering to optimize known tradeoffs between transistor's BVdss and SB voltage to Ron.

Figures 2, 3 show the opposite effects of NDD dosage on Isub and Ron. Isub and Ron are measured as a function of Vgate at Vdrain=20V/0.1V respectively. Isub increases with NDD dosage, while Ron decreases due to the reduction of the serial-resistance of the NDD region.

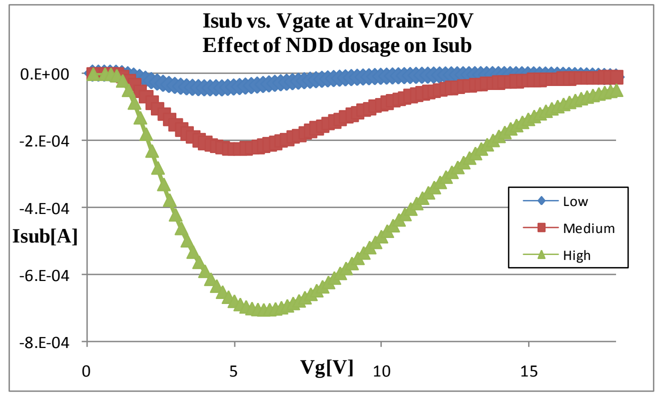


Figure 2 – Isub vs. NDD dosage; Isub increases as dosage increases.

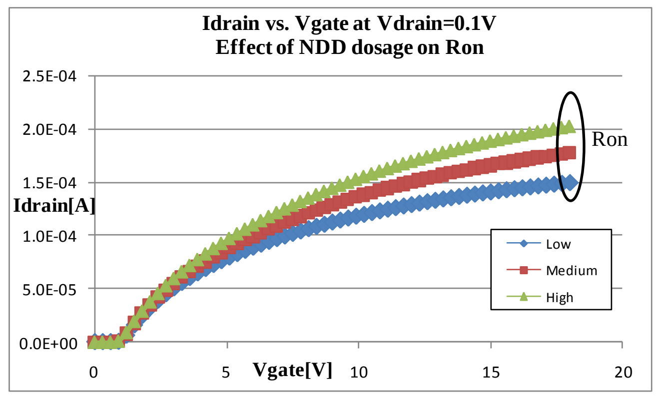


Figure 3 – Idrain vs. NDD dosage; Ron decreases (Idrain increases) as dosage increases.

Despite the increase in Ron, NDD dosage had to be reduced in order to increase SB voltage and diode breakdown voltages.

The n-DEMOS device with a low NDD dosage was subjected to stress at Vdrain=20V and Vgate at maximum Isub. As can be seen in Figure 4, high Idsat and Ron degradation was observed while threshold voltage was not affected, demonstrating that the hot-electron induced degradation was occurring mainly in the NDD region and not inside the channel.

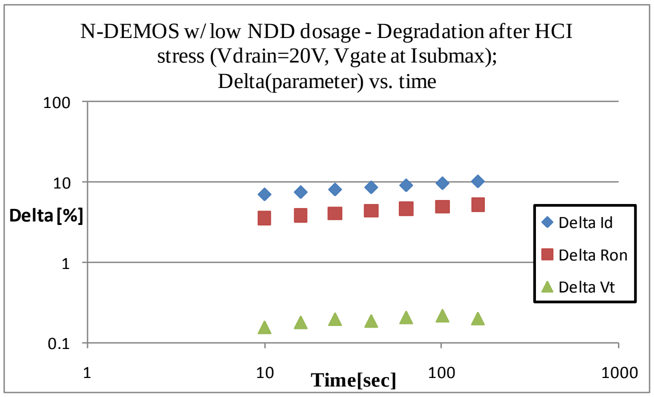
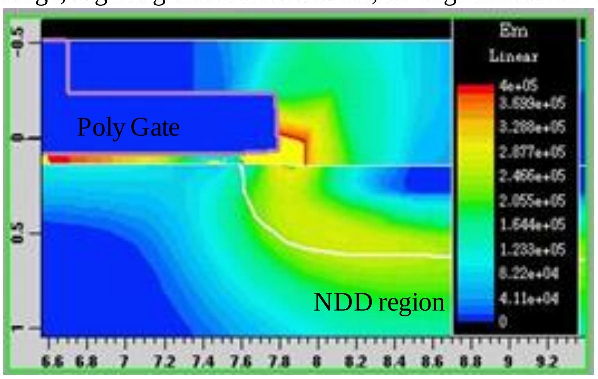
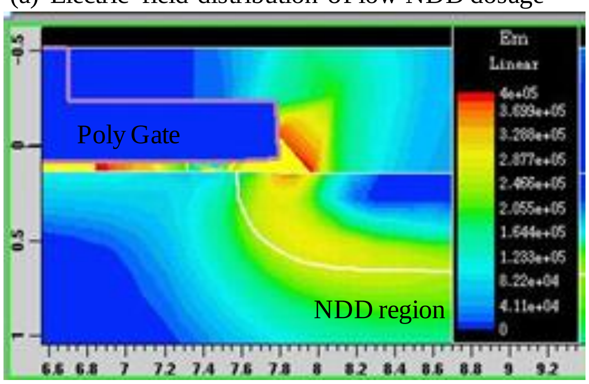


Figure 4 – Degradation after HCI stress for a low NDD dosage; high degradation for Id/Ron, no degradation for Vt.



(a) Electric field distribution of low NDD dosage



(b) Electric field distribution of medium NDD dosage

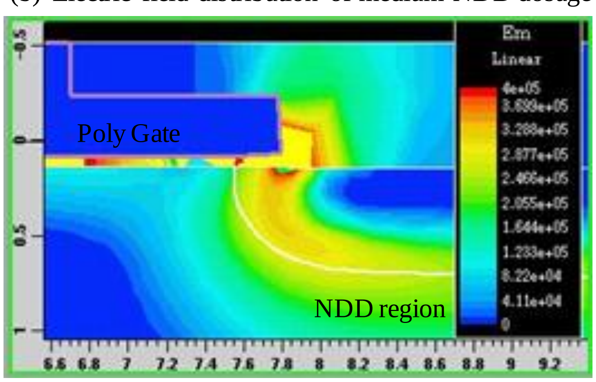
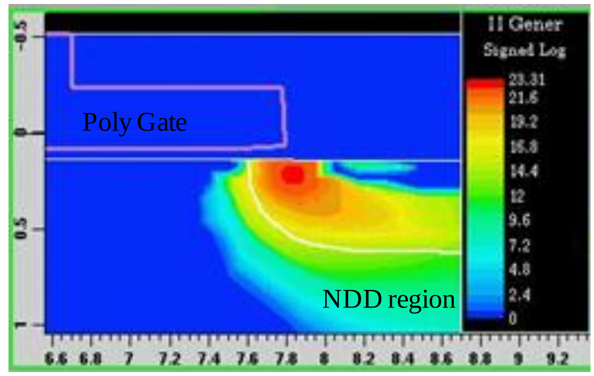
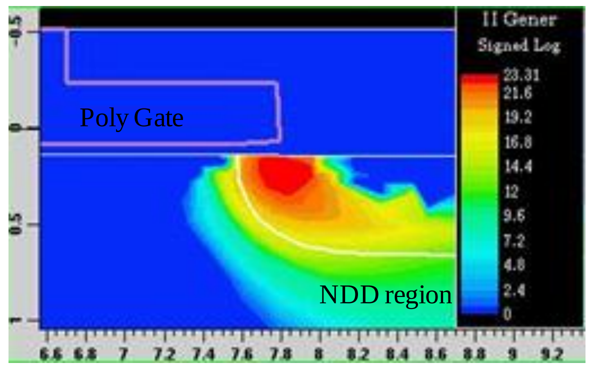


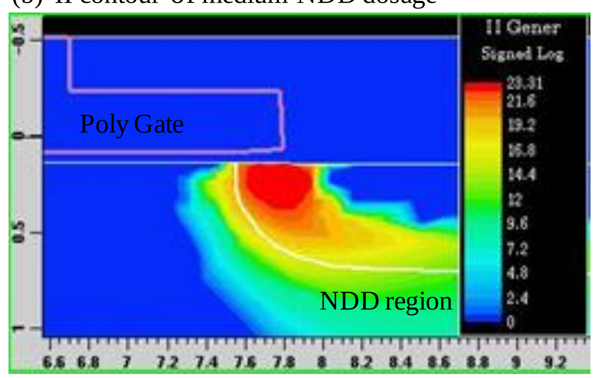
Figure 5 - Electric field distribution as a function of NDD dosage.



(a) II contour of low NDD dosage



(b) II contour of medium NDD dosage



(c) II contour of high NDD dosage

Figure 6 - Contour of Impact Ionization rate as a function of NDD dosage.

Figures 5 and 6 show TCAD simulations of electric field distribution and Impact Ionization pair generation (II) contour as a function of NDD dosage. As can be seen, higher NDD dosage generates higher electric fields and higher II rate. Note that for all dosages, II peak is roughly at the same location in the NDD region in proximity to the gate edge near the surface of the Silicon.

While we expect that higher II rate will increase Isub and Idsat degradation we can see in Figure 7 that higher NDD dosages show lower hot-electron induced degradation.

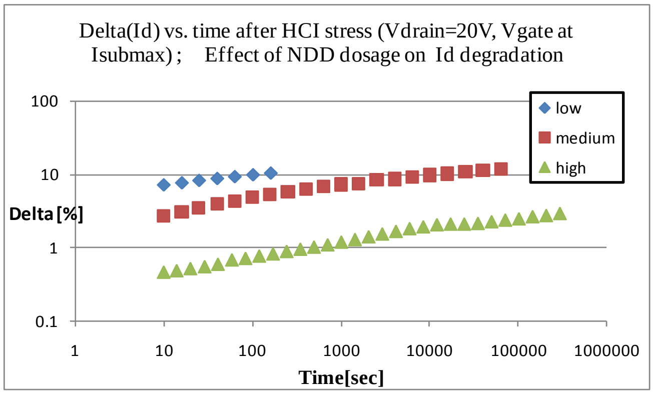


Figure 7 - Id degradation after HCI stress vs. NDD dosage; degradation is decreased as dosage increases.

4. DISCUSSION AND PROCESS OPTIMIZATION

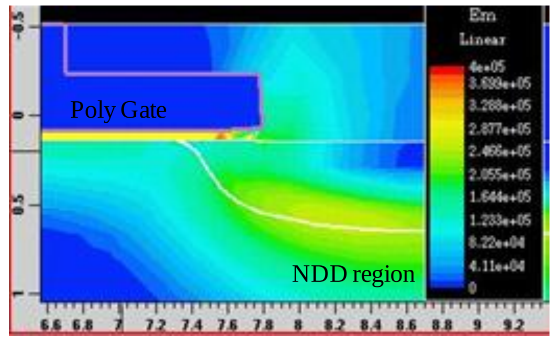
To optimize the tradeoff between the required high SB voltage and low HC degradation which were controlled by the NDD implant a new design parameter had to be introduced.

After examining several options a successful solution was found in the form of Large Angle Tilt implant (LATID). In this approach we tried to shift the peak of electric field downwards from the surface of the silicon and reduce its magnitude, consequently reducing the II rate near the "dangerous" area of silicon surface near the gate *edge*.

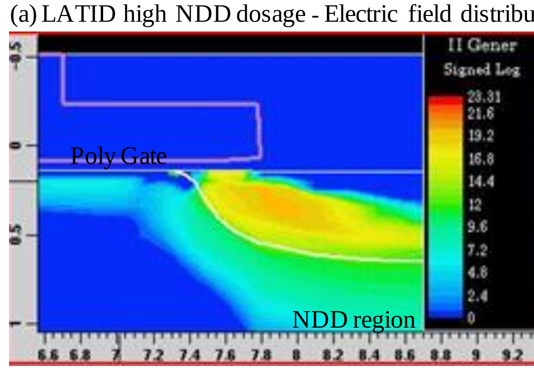
Figure 8 shows TCAD simulations of electric field distribution and II contour of high NDD dosage done at LATID conditions. It can be seen that electric field and II rate are indeed lowered and unlike in the low angle implants, their peaks are located deep inside the silicon and not at the surface.

5. CONCLUSIONS

This paper demonstrates the impact of various NDD dosages on Ron and Idsat degradation in 18V n-DEMOS device, incorporated in 0.6μm platform. Under the same stress conditions, a higher NDD dosage results in a higher substrate current but in a lower Ron and Idsat degradation. We found that using a tilted implant shifts the high electric field away from the dielectric interface, thus suppressing HCI degradation caused by carrier injection into the dielectric and resulting in acceptable device reliability parameters.



(a) LATID high NDD dosage - Electric field distribution



(b) LATID high NDD dosage - II contour

Figure 8 - Electric field distribution and II contour of high NDD dosage done at LATID conditions.

6. REFERENCES

[1] K. M. WU, Jone F. Chen et al, "Anomalous reduction of hot-carrier induced ON resistance degradation in n-type DEMOS transistors", *IEEE Transactions On Device And Materials Reliability", vol. 6, no. 3,* September 2006.
[2] Jone F. Chen et al, "Effect of drift region concentration on hot-carrier induced Ron degradation in nLDMOS transistors", *IEEE Electron Device Letters, vol. 29, no. 7,* July 2008.