DEVICE DESIGN TRADEOFFS FOR 55V LDMOS DRIVER EMBEDDED IN 0.18 MICRON PLATFORM

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ABSTRACT

We describe the optimization of a 55v Breakdown LDMOS embedded in a 0.18 micron based power management platform. The device's self aligned structure allow the accessing low RdsOn values of 50 mohm mm^2. We focus on the effects of gate poly over STI overlap which can increase the breakdown voltage by 10v and reduce maximum substrate current 5 fold while not affecting the specific RdsOn.

Index Terms— Lateral Diffused MOS (LDMOS), Breakdown Voltage (BVDSS), Hot Carrier Injection (HCI), ON Resistance (RdsOn), TCAD

1. INTRODUCTION

Integrated power CMOS platforms combine standard logic with embedded devices capable of switching high currents and voltages. These platforms are proliferating due to the diverse power needs of systems in portable and offline devices. The integration capabilities of embedded platforms allow the reduction of component count on boards integrating digital or analog control circuits with Power management ICs. These are used for applications such as buck/boost converters, LED drivers, and RF power amplifiers.

In 2007, we released a 0.18µm CMOS based Power Management Platform combining dense core logic with integrated power devices with breakdown voltages ranging from 5V to 55V (Fig. 1) [1]. The implementation of high voltage devices in the low voltage platform is realized by using Lateral Diffused MOS (LDMOS) (Fig. 1).

We describe here design tradeoffs between the LDMOS main desired electrical parameters values, namely: (low) RdsOn, (high) source to drain breakdown voltage (BVDSS), (low) Hot Carrier Injection (HCI) degradation, and (high) Snapback voltage. Device optimization is achieved mainly by varying implants and device layout schemes. A significant effect of the poly gate overlap on Shallow Trench Isolation (STI) on BVDSS was observed for 42V LDNMOS deviating from the tradeoff between BVDSS and RdsOn achieved by only varying implant densities. However, increasing the poly overlap also degrades the snapback voltage for high gate voltage. Using TCAD simulations we show that the extended poly length promotes depletion of the drain under off state conditions, but also enhances snapback breakdown in an on state due to a Kirk effect [2]. Consequently, an optimized device layout was chosen and implemented achieving RdsOn of 50 mOhm*mm^2 at a breakdown voltage of 55V.

2. PLATFORM DESCRIPTION

The Integrated power CMOS platform described here is based on Tower's 0.18 micron CMOS process. It comprises of three high voltage deep well implants implemented at the beginning of the process, followed by standard Shallow Trench Isolation (STI) module. CMOS wells are then implanted per process option; post STI deep Nwell implant is optional as well. Single, dual or triple gate oxidations are thermally grown over the wafer depending on process option. Polysilicon deposition and pattering is then performed at the logic & analog parts of the chip. Self-aligned P-type implant is then implanted to form the N-LDMOS body; the implant is self-aligned to the poly at the source side. The process then continues in standard CMOS flow, including extension implants followed by spacer formation. Source & Drain implants, salicide blocking mask, cobalt silicidation, high resistance poly implants as an option and contact module forming the front-end of the wafer. The process flow is schematically described in Fig. 2.

The Backend features up to 6 layers of Aluminum routing metals, including 1.7[fF/µm^2] and 3.4[fF/µm^2] Metal Insulator Metal (MIM) capacitor as an option. In addition to the standard Aluminum 0.9µm top metal one can use either or 2.0µm Aluminum or 3.3µm Copper metallization to allow higher currents and lower metal series resistances.

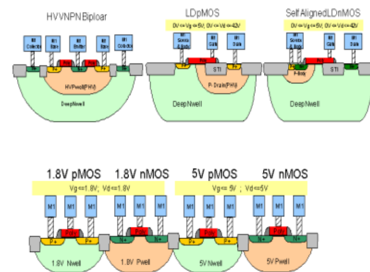

Figure 1: Schematic Cross section of Tower 0.18µm CMOS Integrated Power management platform devices: LDMOS for drivers, CMOS for logic and IO's

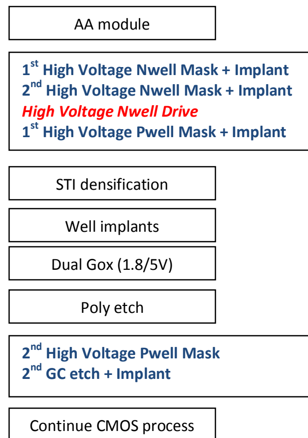

Figure 2: Description of the main steps in process flow for the integrated power CMOS platform

3. EXPERIMENT AND DATA

The 42V LDNMOS (with Breakdown voltage of 55v) in the 0.18 micron platform is described in this paper. Its cross section appears in Fig. 3. The device has a self-aligned body implant which allows the reduction of the device footprint without increasing process sensitivity. Consequently, the self-aligned LDNMOS specific RdsOn per silicon unit area is among the lowest RdsOn values reported.

The device optimization includes a variation of implant doses, conditions and geometric parameters including channel length, STI length, (**s** in Fig. 3) and poly STI overlap (**a** in Fig. 3). The device breakdown voltage is initially set by the dose of the high voltage Nwell implant conditions combined with the **s**. These lead to specific RdsOn and BVDSS values which do not exceed the silicon limit [2].

Once these parameters are set the overlap of the poly on STI, (**a**) is optimized. The poly overlap on STI enhances the depletion of the drain when the device is in the off state. This is accomplished by the large voltage difference between the poly gate held at Vg=0 and the n doped drain which is at high positive voltage. The voltage difference promotes a vertical depletion under the poly which then leads to a lateral depletion from the drain contact to the channel. A full depletion of the drain allows a lower electrical field, for a given s and source drain voltage bias. The overall reduction of the electric field allows accessing higher source drain voltages until a breakdown field is attained. The overall reduced field also suppresses hot carrier degradation effects caused by impact ionization in high fields at the STI edges. Such behavior has been demonstrated on similar structures with dummy gates in [4].

On the other hand a poly edge too close to the drain contact may locally increase the electric field to values exceeding the breakdown field, thus reducing the breakdown voltage.

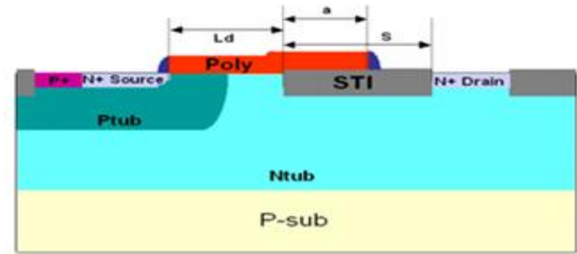

Figure 3: Schematic x-section of the self aligned 42V LDNMOS

In Figure 4 we observe a strong monotonous dependence of BVDSS on **a** with BVDSS varying by 10v (Fig. 4). Consistent with the description above Fig. 5 shows a reduction of the maximum substrate current as function of **a**. Fig. 6 summarizes the variations of BVDSS, RdsOn, and Isubmax with **a**. Note that an increase of **a** reduces Isubmax and enhances BVDSS, both being desirable trends. The variations of **a**, on the other hand, do not affect the device footprint and have a very weak affect on RdsOn.

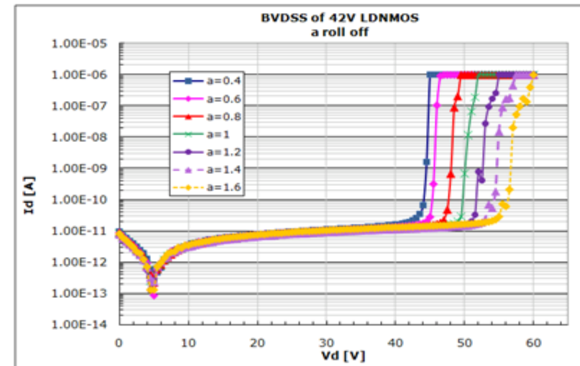

Figure 4: BVDSS of 42V LDNMOS. An improvement of more than 10V is observed for ‘a” ranging from 0.4µm to 1.6µm. In this measurement Vg=Vs=Vb=0v.

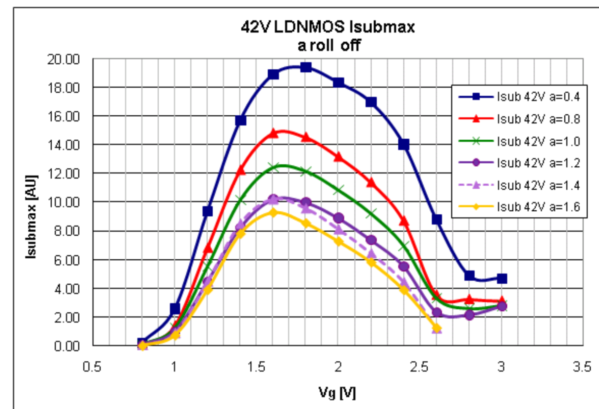

Figure 5: Substrate current as a function of Poly overlap (**a**). A significant improvement in the substrate current is observed. This reduction is then verified by measurements of the hot carrier induced RdsOn degradation.

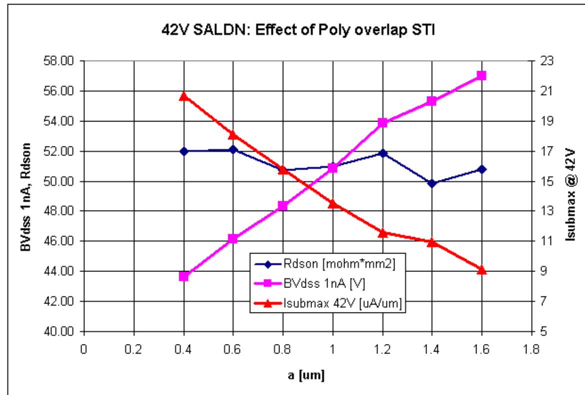

Figure 6: Summary of transistor parameters as a function of **a .**

The improvements in hot carrier HCI degradation performance and BVDSS with **a** are however bounded by other performance factors. Fig. 7 demonstrates that at high gate biases (3V<Vgs<5V) a reduction in snapback voltage is observed for large **a** devices as compared to devices with a shorter **a**. While switch mode operation of an LDMOS driver does not often sample working points with high gate voltage and drain voltages care has to be exercised by design teams to avoid glitches accessing these regimes. Additional drain engineering then alleviates these limitations. Also, as Fig. 8 demonstrates extending **a** beyond 1.6µm reduces the breakdown voltage deviating from the monotonous increase seen at lower **a**.

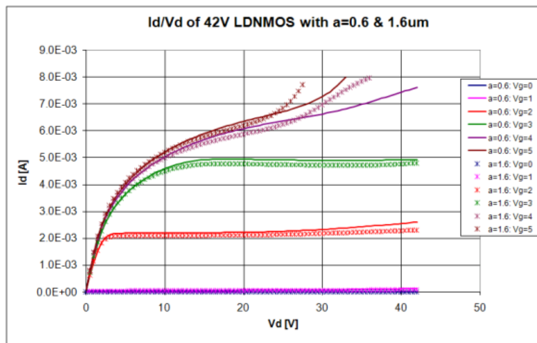

Figure 7: I/V family curves comparing device with a=0.6 & 1.6µm. For Vg>=3V the longer **a** devices have lower snapback voltage.

4. METHOD + PHYSICS MODEL

To understand the silicon results, TCAD simulations were performed for different conditions of gate-source voltage (Vgs) and drain-source voltage (Vds). Two devices were compared with **a**=0.6µm and **a**=1.6µm.

Longer **a** improves the breakdown voltage of the device. During off state, the gate is zero biased or negative in respect to the silicon under STI. This enforces a lower potential on the diffused drain under the STI as seen in Fig. 9 and reduces the maximum electric field as depicted in Fig. 10. The critical field is reached only at higher Vds thus increasing BVDSS.

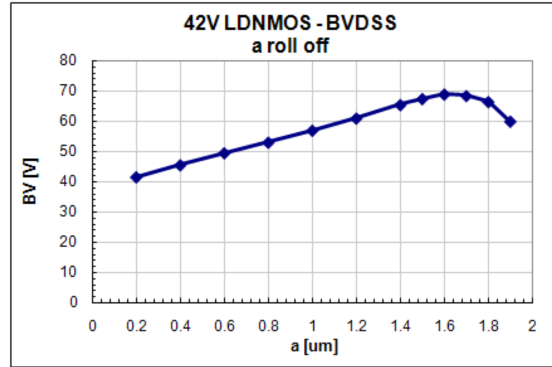

Figure 8: BVDSS dependence on poly overlap for 42V LDNMOS. We can see that BVDSS reaches a maximum value for "a"=1.6µm.

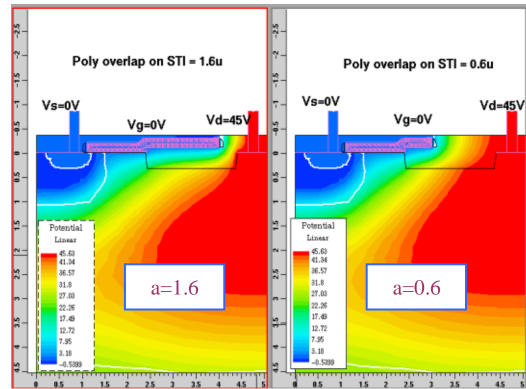

Figure 9: TCAD simulation of potential for two different **a**: 0.6µm and 1.6µm. The potential is lower under the STI for **a**: 1.6µm due to the negative bias from the gate.

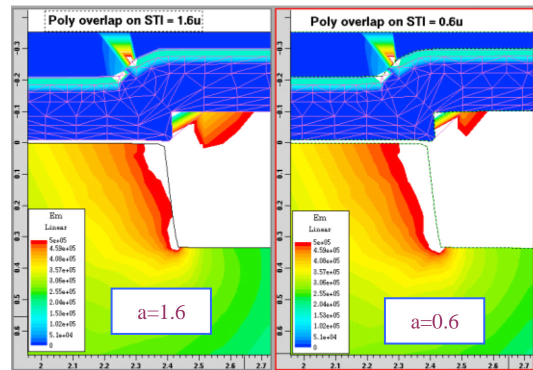

Figure 10: TCAD simulation of Electric field for two different **a**: 0.6µm and 1.6µm. The electric field is more uniformly distributed under the STI.

The reduction of the maximum electric field for larger **a** also improves (suppresses) the HCI degradation. In STI based devices the maximum electric field on the left corner of the STI (Fig. 11 And Fig. 12) leads to high impact

ionization rates. Carriers generated by such process will be trapped in the dielectric layer causing depletion and mobility reduction in the semiconductor. Some common solutions in the literature focus on reducing the consequences of the impact ionization by heavy implants close to the wall of the STI [3] rather than suppressing the impact ionization itself (by reducing the maximum electric field). In the work described here, the extension of **a** directly reduces the carrier generation by impact ionization. A closer look at the left corner of the STI (Fig. 11) shows how the electric field is weaker causing less impact ionization for a given drain voltage and improving HCI degradation.

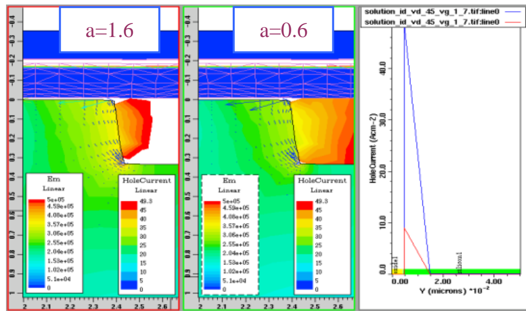

Figure 11: Zoom of left corner of TCAD simulation of Electric field for two different **a**: 0.6μm and 1.6μm for Vgs=1.7V and Vds=45V

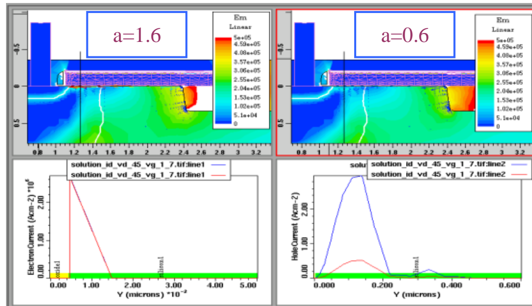

Figure 12: TCAD simulation of Electric field for two different **a**: 0.6μm and 1.6μm for Vgs=1.7V and Vds=45V in the body region close to the channel.

We now address the reduction of the snapback voltage for longer **a** devices.

For high voltage gate, the electron current injected in the drift resistor is no more considered as a weak injection. The electron concentration is now higher than the doping concentration of the drift region and should be taken into account in the Poisson equation. This Kirk effect has been noted by others [6-7] and for this device geometry causes a second peak of the electric field at the right STI edges: An extended gate promotes a large electron accumulation layer under the STI which does not allow high voltage gradients along the STI silicon interface. Consequently a second high gradient (electric field) region develops on the right corner of the STI near the drain contact. As TCAD simulation confirm (Figure 13, 14) at high gate biases, for large **a** devices strong fields develop at the right edge of the STI (near the drain contact). Consequently holes generated at that edge promote snapback behavior.

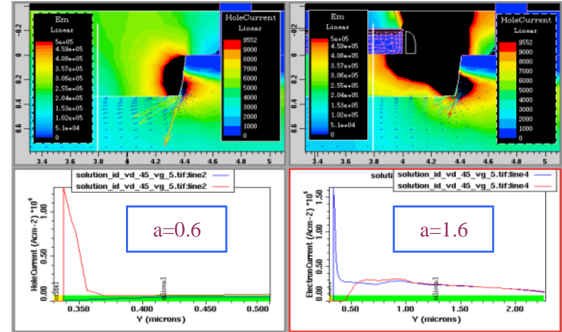

Figure 13: TCAD simulation of Electric field for Vgs=5V and Vds=45V on the right corner of STI with holes-electrons current. The higher field on the corner causes a higher level of impact ionization, generating much more pairs of electrons-holes.

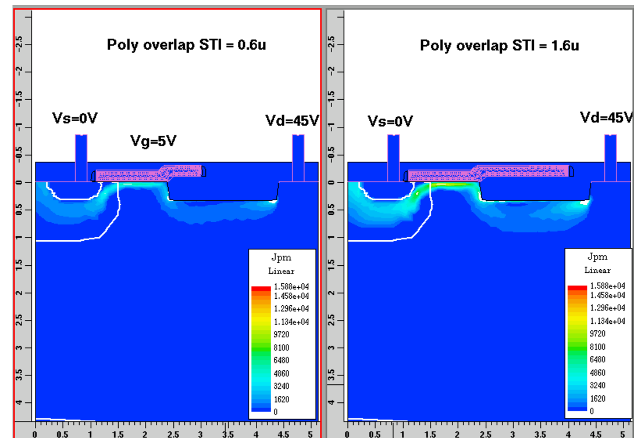

Figure 14: TCAD simulation of Hole currents for two different **a**: 0.6μm and 1.6μm for Vgs=5V and Vds=45V . One can observe the higher hole currents generated in the right STI edge for longer **a** aggravating snapback effects.

The alleviation of the Kirk effect can be addressed by intermediate doping around the drain contact.

5. SUMMARY

We have presented a review of the optimization of the 42V LDNMOS in an integrated power CMOS platform. The tradeoff between the main desired electrical parameters namely: (Low) RdsOn, (high) BVDSS, (low) HCI degradation, and (high) Snapback voltage was presented. Focusing on the effect of of poly overlap on STI we found that a longer overlap allows a gain of 10V in BVDSS without effect on the RdsOn of the device. However it also

degrades the device SOA with higher snapback for high gate voltage. This is demonstrated by measurement data and TCAD simulations. It was clearly shown that the extended poly length promotes depletion of the drain in an off state but also enhances snapback breakdown in an on state due to a Kirk effect. The alleviation of this effect can be addressed by intermediate doping around the drain contact.

6. REFERENCE

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