

# INTEGRATED 0.18 MICRON RF TECHNOLOGY PLATFORM WITH 1.8V 5V 12V 25V & 42V MOS FOR HIGH DIGITAL CONTENT POWER RF APPLICATIONS FEATURING $f_T = 55$ GHZ RFMOS AND $f_T > 17$ GHZ 12V RF-LDMOS.

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## Abstract

Tower's 0.18 micron RF CMOS Power integrated circuit platform is described. The platform includes a 0.18 micron based core logic process with embedded 1.8v RFMOSFETS featuring an  $f_T=55$ GHz and  $f_{max}=70$ GHz. To surpass the power limit of ~30 dbm achievable with a standard 1.8v / 3.3v platform, embedded RFLDMOS devices with a 23V breakdown voltage rating are developed. Thick 3.3 $\mu$ m Copper top routing or 2.2 $\mu$ m Aluminum are added to allow large currents and as a quality enhancer for top metal inductors. Integrated RF components such as MOSFETs, Varactors, metal Capacitors, Inductors and Schottky diodes are all optimized for RF performance. The platforms capabilities were demonstrated by designs of a 24GHz LNA and a 5GHz dual channel MIMO transceiver.

In addition the platform can support lower frequency power management applications. A 12V integrated LDMOS with  $R_{dson}$  of 10.7[m $\Omega$ \*mm<sup>2</sup>] and Low  $R_{dson}$  25V and 42V LDMOS transistors are embedded and may be used, as power switches in PM applications. Complimentary devices and circuits such as HV ESD, HV Schottky diodes, HV & high gain Bipolars are also integrated to allow analog design. A 25V 2A DC-to-DC buck-boost circuit was designed and tested on silicon to demonstrate the platform power management capabilities.

## Introduction

The reduction of transistor size on silicon based Integrated circuits has allowed integrated RF transceivers to become a system on chip integrating both heavy digital content and analog RF functions. In doing so silicon is replacing SiGe, GaAs and Other III V materials as the platform of choice for RFIC applications.

As scaling continues MOSFET unity current and power gain frequencies,  $f_T$  and  $f_{max}$ , are rising [4]. Nevertheless current platforms are capable of transmitting power in the range of 30 dbm limited primarily by low current densities which the platform allows. When larger power output is needed one applies higher voltage discrete devices such

as in base station applications. To break the power output barrier one needs to integrate high voltage / high frequency devices in an advanced CMOS platforms and enhance the platforms current carrying capacity. Such an integration scheme allows higher RF power outputs. Thus the RFCMOS platform is now relevant to applications such as cellular phone power amplifiers, which have so far utilized GaAs and SiGe platforms. The enhanced capabilities of the CMOS platform also enable it to enter new low frequency applications such as voltage converters, audio amplifiers, display drivers and other high voltage applications.

## **1. Process Flow**

The RF Power integrated platform describe here is based on Tower's 0.18 micron CMOS process. It comprises of high voltage deep well implants implemented at the beginning of the process, followed by standard Shallow Trench Isolation (STI) module. CMOS wells are then implanted per process option, post STI deep Nwell implant is optional as well. Single, dual or triple gate oxidations are thermally grown over the wafer depending on process option, Polysilicon deposition and patterning is then performed at the logic & analog parts of the chip. Self-aligned P-type implant is then implanted to form the N-LDMOS body, the implant is self-aligned to the poly at the source side. The process then continues in standard CMOS flow, including extension implants followed by spacer formation. Source & Drain implants, salicide blocking mask, cobalt silicidation, high resistance poly implants as an option and contact module forming the front-end of the wafer.

The Backend features up to 6 layers of Aluminum routing metals, including  $1.7[\text{fF}/\mu\text{m}^2]$  and  $3.4[\text{fF}/\mu\text{m}^2]$  MiM capacitor as an option. In addition to the standard Aluminum  $0.9\mu\text{m}$  top metal one can use either or  $2.0\mu\text{m}$  Aluminum or  $3.3\mu\text{m}$  Copper metalization to allow higher currents and lower metal series resistances.

## **2. Low Voltage MOS Transistors**

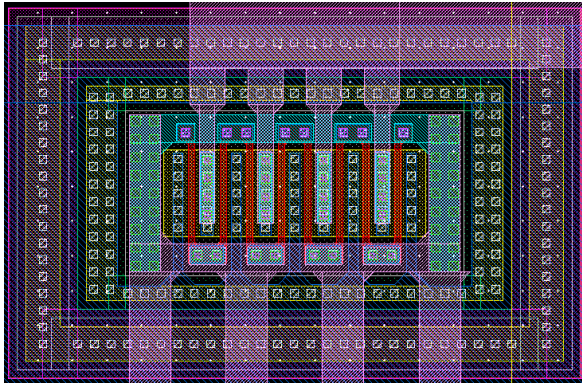
Low voltage RF transistors shown in Table 1 are carefully designed to optimize the high frequency characteristics such as  $f_t$ ,  $f_{\text{max}}$  & noise. Special care was taken during the layout of these transistors to minimize gate resistance and parasitic capacitances, specifically the gate to drain capacitance. Figure 1 shows a layout of an RF NMOS. The transistor's gate electrode is fingered to minimize gate resistance. For the same reason each of the poly gate fingers is connected on both sides.

RF-NMOS transistors may be drawn inside deep Nwell (optional) for isolation from the P-substrate, by that the transistor is less subjected to substrate noise.

LV RF-MOS transistors are scalable in channel width, channel length & number of gate fingers, allowing the flexibility to choose an optimized device in terms of gain, noise and power consumption.

Device	L-drawn [um]	V <sub>GS</sub> [V]	V <sub>DS</sub> [V]	V <sub>th</sub> [V]	I <sub>dsat</sub> [uA/um]	BV <sub>dss</sub> [V]	R <sub>dson</sub> [mΩ*mm <sup>2</sup> ]	F <sub>t</sub> [GHz]
1.8V n/p MOS	0.18/0.18	1.8	1.8	0.42/-0.50	600/260	>3.6		55/23
3.3V n/p MOS	0.35/0.30	3.3	3.3	0.72/-0.68	600/300	>6.0		22/14
5.0V n/p MOS	0.60/0.50	5.0	5.0	0.85/-0.80	550/300	>7.0	2.1/5.8	

**Table -1.** Characteristic parameters of the low voltage MOS transistors.



**Figure 1.** Layout view of LV RF-NMOS transistor, the transistor is isolated from the P-substrate by a deep Nwell (outer ring) to suppress substrate noise. Poly, drawn in red, is connected by M1 on both sides.

### 3. High Voltage MOS transistors

Lateral Diffused MOS transistors are integrated to the CMOS platform to allow higher RF power output as well a low frequency power management applications. The transistors are optimized for low R<sub>dson</sub> & high breakdown voltage when used as power switch. When used in RFIC as the building blocks for power amplifiers the layout and process optimization is focused on maximizing gm while minimizing capacitances and gate resistance.

Our platform offers LDMOS devices ranging from 12V to 42V drain operating voltage and 3.3V or 5V gate voltage (Table 2), with breakdown voltages targeted 30% above the operation voltage. Figure 2 shows a schematic cross section of different LDMOS transistors available at the process [5], [6].

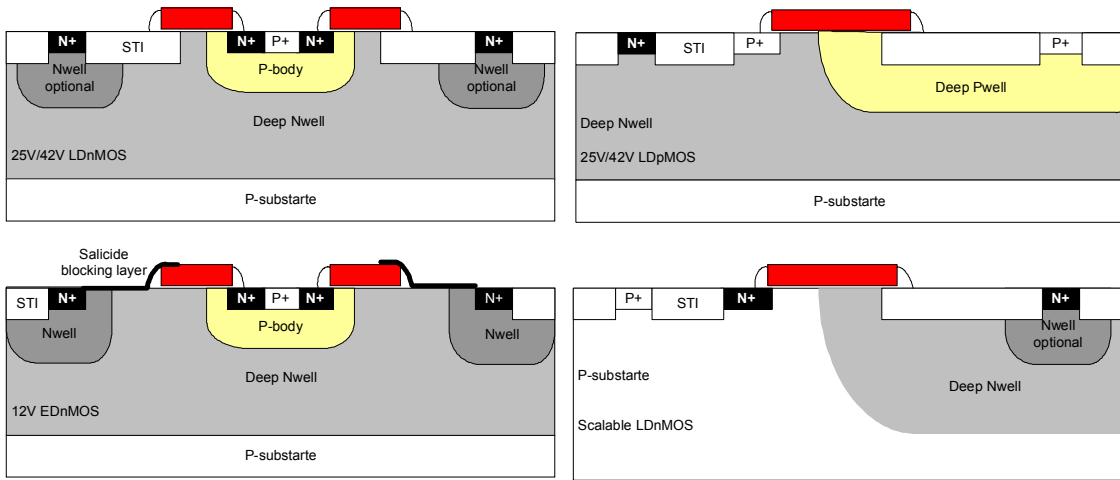
A self-aligned body implant allows the reduction of the device footprint without increasing sensitivity to process. Consequently the specific R<sub>dson</sub> per silicon unit area of the self-aligned LDNMOS are among the leading results reported. Device breakdown voltage is controlled by the space between the Nwell covering the N+ drain to the channel, this allows different voltage rating transistors to coexist on the same wafer without additional processing.

In addition to the RF and switch mode LDMOS transistors, which are fixed in channel length, the platform provides a set of scalable length LDMOS transistors. These devices exhibit allow high voltage analog design, where matching and output resistances are most important parameters.

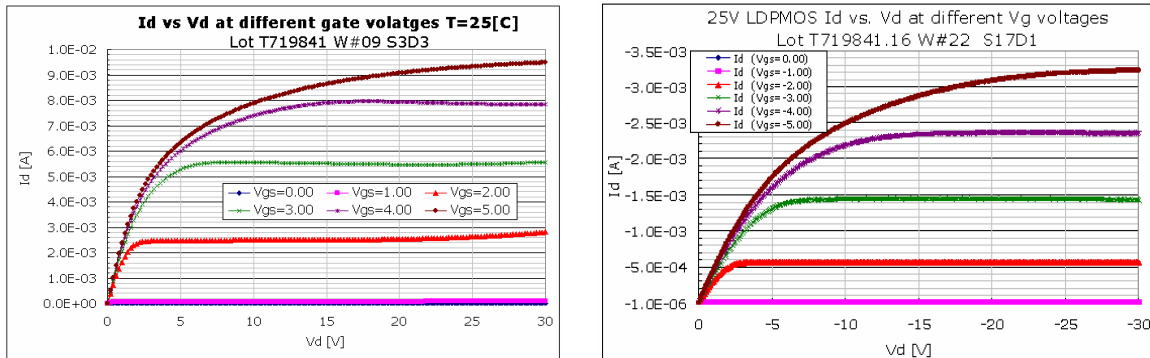
Figures 3 showing typical I/V curves of 5V gate 25V drain LDMOS transistors. The devices shows good immunity to snapback even at 30V.

Device	V <sub>GS</sub> [V]	V <sub>DS</sub> [V]	V <sub>th</sub> [V]	I <sub>dsat</sub> [uA/um]	BV <sub>dss</sub> [V]	R <sub>dson</sub> [mΩ*mm <sup>2</sup> ]	F <sub>t</sub> /F <sub>max</sub> [GHz]
12V n LDMOS	5.0	12	0.78	610	23	10.7	17.3/27
25V n LDMOS	5.0	25	0.87	510	34	28	
42V n LDMOS	5.0	42	0.95	340	52	55	

**Table -2.** Characteristic parameters of LD-nMOS transistors.



**Figure 2.** Schematic cross sections of 25V, 42V self-aligned LDnMOS (upper left) a 12V self-aligned EDnMOS (bottom left), scalable LDpMOS (upper right) and a scalable LDnMOS (bottom right)



**Figure 3.** Drain current vs. drain voltage curves of 5V gate & 25V drain NLDN MOS (left) and PLDMOS (right).

#### 4. Passive Components

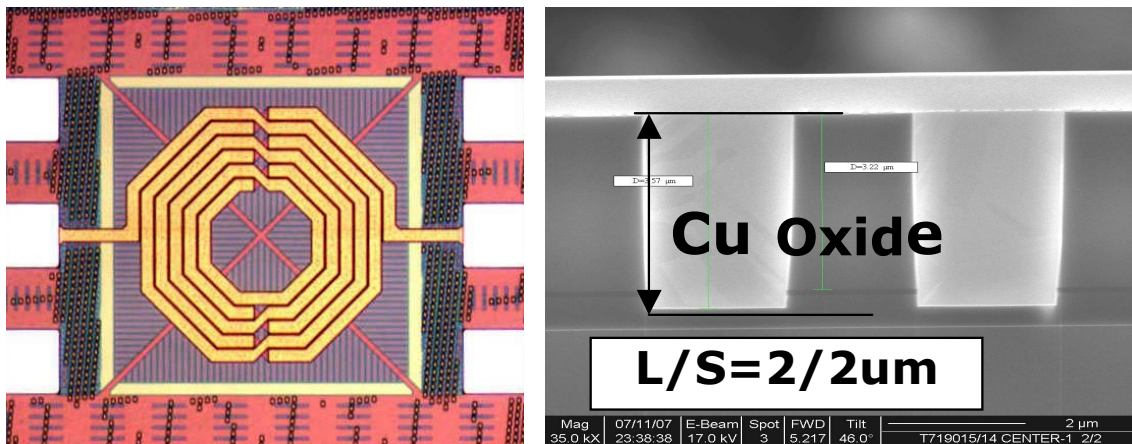
To allow RFIC System On Chip design, passive components are added to the pdk. Integrated planar inductors, usually having the lowest quality factor among passives due to the conducting substrate and metal resistance, pose a great challenge to the process, device & design teams. Different types of inductor layouts are supported for easiness of design. Fig 4 shows a top view of a symmetrical inductor with thick top metal and patterned ground. Poly silicon & first metal are used for screening the electric field from penetrating the substrate therefore increasing the quality factor at expense of lower self resonance frequency. The Inductor is formed either by connecting different metal levels in parallel for reducing resistance or by using one of the thick metal options the process allows.

Power management application require a thick top metal routing to pass the large currents through the switching transistor, in this platform a 3.3um thick Copper metal, with sheet resistance of 6.5[m $\Omega$ /sq], is integrated on top of the Aluminum backend, the metal is also used for high Q inductors.

Transmission lines allowing designs at frequencies above the typical resonance of inductors have been used in a 24GHz LNA design with gain of 13.4db and noise figure of 2.8 and demonstrated on silicon [1].

The platform offers a portfolio of passive capacitors. The 1.8V MOS Varactors allow the highest capacitance density, 10 [fF/um<sup>2</sup>]. The capacitance, however, varies significantly with voltage and has low voltage bias limits identical to the MOS transistor.

Backend capacitors on the other hand, such as Metal Insulator Metal (MIM), have very small voltage and temperature dependence, higher quality factor and higher operating voltage range.



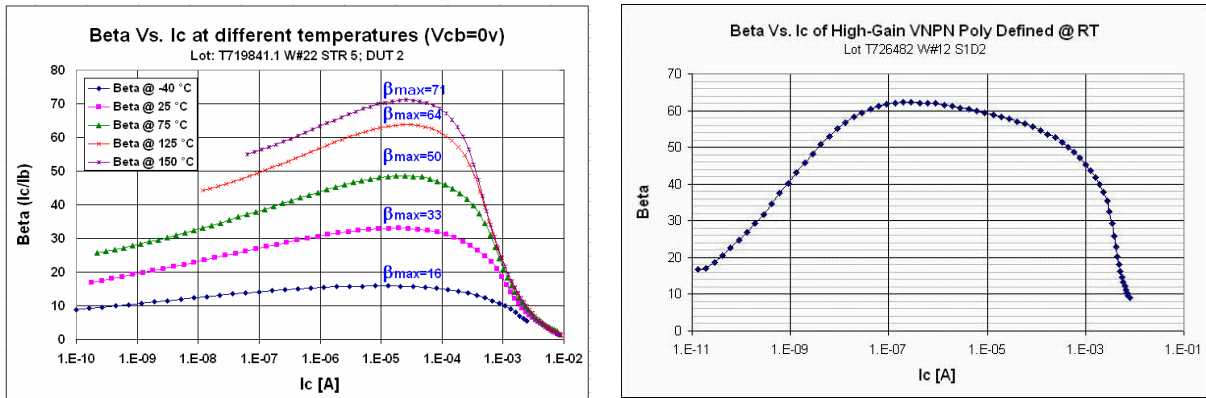
**Figure 4.** (Left) top view picture of a symmetrical inductor test structure with patterned ground connected through GSG pads. (Right) SEM X-section showing thick Copper layer.

Schottky diodes, usually the device of choice for rectifying small signal from the antenna in RFID passive tags, are also included in the kit. The diode is formed of CoSi contacting a low-doped P-type silicon, it is realized without adding any processing steps. Diodes have low barrier of 330mV (which can be tuned by implants) and cutoff frequency above 90GHz, which enables high rectification efficiency.

## 5. Bipolar Transistors

Bipolar transistors commonly used in band gap references or differential amplifiers are part of the platform. Apart from the CMOS parasitic Bipolars, an improved performance set of devices is engineered to allow the design of high voltage analog circuits. HV NPN and PNP transistors realized using the existing masks adding no extra processing steps, show gains of 33 & 90 BV<sub>ceo</sub> of 11V & 40V and early voltages of 320V & 150V respectively.

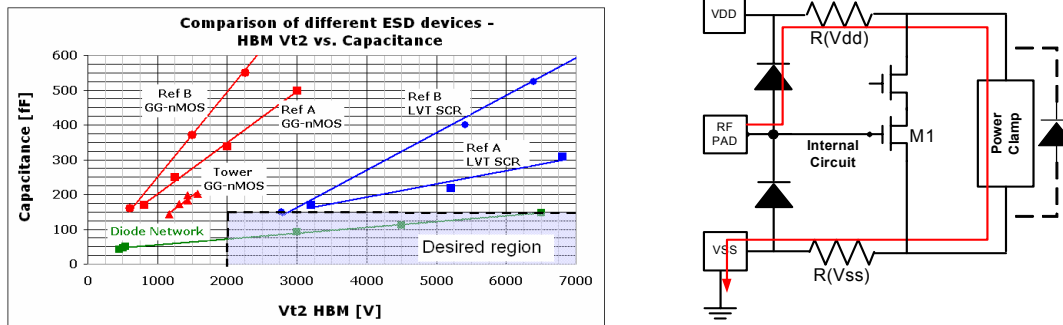
In addition to the standard process high voltage bipolar transistors described above, a high gain low voltage bipolar transistor (figure 5) may be implemented by adding a implant step. The resulting device has a current gain higher than 60 and early voltage above 12V.



**Figure 5.** Left - Current gain vs. Collector current of an HV vertical NPN bipolar  
Right - Current gain vs. Collector current of an LV high gain vertical NPN

## 6. I/O and ESD devices

I/O and ESD protection circuits for the digital & analog pads are part of the standard offering, there are multiple cells supporting different input and /or output pads. Protection circuits for RF pad have unique characteristics that have to be met. The input capacitance has to be as small as possible (less than 150fF for most silicon applications) with minimum compromising on the ESD protection. At the same time serial resistance between pad and transistor gate has to be as low as possible in order not to add noise at the LNA input.



**Figure 6.** Left - capacitance vs. HBM rating of different ESD solutions, showing the superiority of diode network. Right – schematic of diode network protection circuit showing a worst case ESD event between RF pads to Vss.

A diode network (Figure 6) is a common practice solution. It provides a better capacitance to ESD robustness ratio compared with other common solutions such as SCR or GG-NMOS [7]. The diode network is comprised on two shunting diodes, one from pad to Vss other from pad to Vdd. ESD protection diode with scalable length is integrated to allow trade offing of capacitance with protection level. Power clamps used to shunt the ESD current between different power rails are standard cells in the pdk.

Protection over HV pads is achieved by either an RC detection circuit triggering an active LDMOS clamp or by HV-SCR, while the 1<sup>st</sup> is easier to design it consumes larger area.

## 7. Conclusions

Integrated RF Power platform based on Tower's 0.18 $\mu$ m CMOS was introduced, the platform integrates LV MOS transistors for logic, analog and RF design. HV LDMOS transistors with low R<sub>dson</sub>, ranging from 12 to 42V can support both power and RFIC applications. In additions scalable length LDMOS transistors are included to enhance analog characteristics of the device.

Passive components such as thick metal Inductors, Varactors, MiM capacitors and Schottky diodes are all part of the platform.

Bipolar transistors with enhanced performance are integrated to support analog design where either high voltage or high gains are needed. Finally different ESD solutions to protect the RF & HV pads are discussed.

## 8. References

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