

# A Physically Based, Scalable MOS Varactor Model and Extraction Methodology for RF Applications

James Victory, *Senior Member, IEEE*, Zhixin Yan, *Member, IEEE*, Gennady Gildenblat, *Senior Member, IEEE*, Colin McAndrew, *Fellow, IEEE*, and Jie Zheng

**Abstract**—A physically based scalable model for MOS varactors, including analytical surface potential based charge modeling and physical geometry and process parameter based parasitic modeling, is proposed. Key device performances of capacitance and quality factor  $Q$  are validated over a wide voltage, frequency, and geometrical space. The model, implemented in Verilog-A for simulator portability, provides for robust and accurate RF simulation of MOS varactors.

**Index Terms**—MOS varactors, surface potential, VVCs.

## I. INTRODUCTION

ACCUMULATION-MODE MOS varactors built in standard CMOS or BiCMOS technology have emerged as the primary frequency tuning device for RF applications such as voltage-controlled oscillators (VCOs) [1]–[4]. As technology dimensions and supply voltages continue to decrease, MOS varactors provide higher quality factor and extended tuning range, compared to junction diode varactors, in the GHz range [1]–[4]. Additionally, MOS varactors are free for any given CMOS or BiCMOS technology in that there are no extra masks required to build the device. In modern technologies, the tuning range offered by the standard source and drain junction varactors is not adequate for VCO applications. Therefore, special implanted junction varactors are created to enhance the tuning range at the typical cost of an extra mask. Given the performance advantages and cost, the MOS varactor is the device of choice for tuning applications in many instances.

Prior modeling of MOS varactors is predominantly subcircuit treatments of the device which include the intrinsic capacitance through either a MOSFET (BSIM) element or a polynomial behavioral equation. Device parasitic resistance, capacitance and inductance are conventionally included through lumped treatments and device performances are validated over a small geometry and frequency space. The BSIM or any MOSFET model assumes frequency independent inversion charge sources supplied from the source and drain. Without source and drain regions, the inversion charge in an accumulation-mode MOS varactor is frequency dependent since it is thermally generated. In [5], the BSIM model generates the capacitance–voltage ( $C$ – $V$ ) characteristics by floating the source and drain regions to force

a depletion capacitance characteristic. Since the BSIM model uses separate equations for the MOS charge in accumulation and depletion, care must be taken to avoid unphysical kinks in the  $dC/dV$  characteristics as shown in [5]. Third-order voltage related polynomial expressions are used in [6] to model both  $C$ – $V$  and quality factor–voltage ( $Q$ – $V$ ) characteristics of a MOS varactor. The work in [7] presented physical models for the device resistance but relies on polynomial capacitance modeling.

This paper advances the state of the art by providing for the first time a completely physically based MOS varactor model including the intrinsic charge and parasitic components. This physically based platform for modeling lends itself to robust statistical modeling [8]. The frequency dependent MOS capacitance model in [9] is advanced based on an analytical solution to the frequency dependent surface potential. Robust extraction procedures for predominantly process and geometry based parameters across a wide geometry, bias, and frequency space are presented. The proposed model is implemented in Verilog-A to provide portability among various simulators.

In Section II, the MOS varactor device is presented. Section III presents the critical frequency dependent, surface potential based model for the intrinsic charge which leads to accurate intrinsic capacitance simulation. The modeling of the device parasitics, which include resistance, inductance and capacitance, is presented in Section IV. Section V details the parameter extraction procedure and playbacks of the model to measured results.

## II. DEVICE TECHNOLOGY AND LAYOUT

Fig. 1 shows a cross section view of the standard MOS varactor offered in CMOS and BiCMOS technologies. The figure illustrates the accumulation (left side) and depletion (right side) regions of operation. The device is formed by replacing the  $P^+$  source, drain, and poly implants of a PFET device with  $N^+$  implants, thereby providing direct contact to the NWELL under the poly gate. The advantage of this configuration is the self alignment of the  $N^+$  contacts to the poly gate, allowing small gate lengths. The  $N^+$ –poly/NWELL combination roughly centers the  $C$ – $V$  characteristics on the  $V_{GB} = 0$  axis. In some cases, a design calls for the  $C$ – $V$  characteristic shifted to the positive  $V_{GB}$  axis. In this case, the poly gate is doped  $P^+$  which could result in an added mask and increased minimum channel length to allow for proper separation of the  $P^+$  to the  $N^+$  NWELL contact. The NWELL is almost always used for the bulk region for reasons of lower resistance and improved substrate isolation compared to a PWELL. For these reasons, the  $N^+$ /NWELL device is most common. The bulk of the modeling work in this paper

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J. Victory, Z. Yan, and J. Zheng are with Jazz Semiconductor, Newport Beach, CA 92660 USA.

G. Gildenblat is with The Pennsylvania State University, University Park, PA16802 USA.

C. McAndrew is with Freescale Semiconductor, Tempe, AZ 85284 USA.  
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where  $u_0 = \psi^{(0)}/\Phi_t$ ,  $u = \psi/\Phi_t$ , the thermal potential is  $\Phi_t = kT/q$ , and  $\gamma = \sqrt{2q\epsilon_{\text{Si}}N_b}/C_{\text{ox}}$  denotes the body factor dependent on surface doping  $N_b$  and  $C_{\text{ox}}$ . Note that the sign convention is such that all charges are negative in the depletion and in the inversion regions for an NWELL device. We note in passing that except for the exponential terms (6) and (7) coincide with the results of the standard depletion theory. Inclusion of the exponential term accounts for the contribution of the majority carriers and is essential in the accumulation region and close to the flat-band voltage [12].

A common difficulty of any surface-potential-based model is the computation of  $\psi^{(0)}$  as a function of the gate bias  $V_{\text{GB}}$ . The implicit  $\psi^{(0)}(V_{\text{GB}})$  dependence is given by

$$\begin{aligned} & (V_{\text{GB}} - V_{\text{FB}} - \psi^{(0)})^2 \\ & = \gamma^2 \Phi_t \{ \exp(-u_0) + u_0 - 1 + \Delta [\exp(u_0) - u_0 - 1] \} \end{aligned} \quad (8)$$

where

$$\Delta = \exp\left(-2\frac{\Phi_F}{\Phi_t}\right) \quad (9)$$

and  $\Phi_F$  denotes the so-called Fermi potential [12], [13].

Traditionally (8) is solved iteratively using the Newton–Raphson method with a suitably chosen initial guess [9], [14]. More recently, several analytical (noniterative) approximations have become available [15], [16]. In particular, the approximation developed in [16] and extended in [10] to include all regions of MOSFET operation has the accuracy of at least 1 nV and is sufficiently well-behaved to allow one the computation of the derivative, i.e., of the quasi-static capacitance

$$C = C_{\text{ox}} \left( 1 - \frac{d\psi^{(0)}}{dV_{\text{GB}}} \right). \quad (10)$$

It is this approximation that is used to obtain  $\psi^{(0)}(V_{\text{GB}})$  dependence in the present paper.

We now turn to a different problem of computing the actual, nonquasi-static surface potential assuming that both the inversion charge and the gate bias are known. This computation is essential for the relaxation time method in the form developed in [9] where it is shown that

$$(V_{\text{GBI}} - V_{\text{FB}} - \psi)^2 = \gamma^2 \Phi_t [u - 1 + \exp(-u)] \quad (11)$$

and

$$V_{\text{GBI}} = V_{\text{GB}} - q_i. \quad (12)$$

The approximate analytical solution of (11) is based on the observation that it can be formally obtained from (8) by changing  $V_{\text{GB}}$  into  $V_{\text{GBI}}$  and setting  $\Delta = 0$ . In other words,  $\psi$  satisfies the same equation as the surface potential of the MOS capacitor with the gate drive  $V_{\text{GBI}}$  and the minority carrier contribution to the space charge turned off. The latter problem has already been considered in [17] in connection with the modeling of the source/drain overlap regions (surface potential-based modeling of the overlap regions has been first developed within the context of the MM11 model [11] using iterative computation of the

surface potential). The corresponding analytical approximation [17] has an excellent accuracy (typically 0.1 nV) and is obtained by simplifying the original work in [16] by neglecting the minority terms and optimizing some intermediate steps. Since the presentation of this approximation in [17] contains several misprints, the corrected equations are detailed here in the Appendix.

Once  $\psi$  is computed, (5) can be used to obtain the gate charge and hence MOS  $C$ – $V$  characteristic. Numerically, the use of the analytical approximations for  $\psi^{(0)}$  and  $\psi$  is inconsequential so the simulation results presented in [9] and in the present paper remain unaffected by this change of the computation algorithm. However, the elimination of two iteration loops improves both the convergence and the computational efficiency of the relaxation time approximation, model evaluation time is approximately halved with the switch from iterative to analytical solutions.

Implementation of models in circuit simulators, including manual generation of derivatives, is a tedious and error-prone process, and generally specific code is required for each simulator in which a model is implemented. To significantly speed up model implementation time, to eliminate the need to hand generate and code derivatives, and to allow portability across simulators, we have implemented our model in the standard Verilog-A language. Added benefits of this approach are that the complete code for the model is in a single place, rather than being spread across multiple routines and files, and that it makes it easy to pass code back and forth between multiple model developers.

The implementation is primarily done using voltage controlled current contribs (a contrib is a branch contribution to the equivalent network representation of a model defined in Verilog-A) and voltage controlled charge elements, which become current contribs via the  $ddt()$  time derivative operator. The frequency dependence of the capacitance is not implemented directly, but follows implicitly from the Verilog-A implementation of the model described above. From the voltage across the capacitor, the quasi-static values of the surface potential  $\psi^{(0)}$  and inversion charge  $q_i^{(0)}$  are calculated. Equation (1) is solved by introducing an internal node in the model, the voltage on that node being  $q_i$ , and then summing contribs at that node to represent (1), rewritten as

$$q_i = q_i^{(0)} - \tau \left( \frac{dq_i}{dt} \right). \quad (13)$$

The equivalent network is simply a 1-Ohm resistor (the  $q_i$  term), a capacitor of value  $\tau$  (the  $\tau^* ddt(q_i)$  term), and a current contrib of the calculated  $q_i^{(0)}$ . This implicit representation of the model is solved self-consistently within the circuit simulator. Equation (11) is solved directly for  $\psi$ , knowing  $q_i$ , and the charge is calculated from (5). The  $ddt()$  contrib of this charge represents the frequency and bias dependent core MOS varactor capacitance.

At low frequencies (relative to  $1/\tau$ )  $q_i$  tracks  $q_i^{(0)}$  and so the solution for  $\psi$  is equivalent to that of the quasi-static formulation (8). The  $C(V)$  curve then follows that of a MOSFET, where in strong inversion the capacitance is determined by charge balance between the gate charge and the inversion charge. For fre-

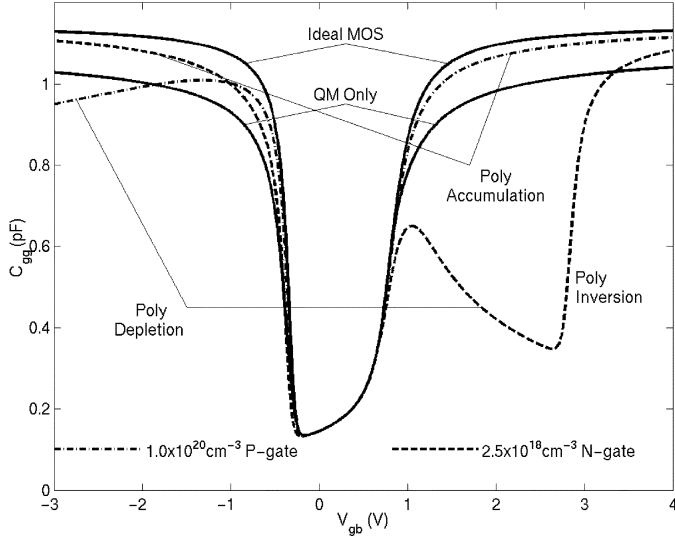


Fig. 3. Simulation of MOS  $C-V$  characteristics including quantum (QM) and polysilicon doping (PD) effects.

quencies high with respect to  $1/\tau$ ,  $q_i$  becomes pinned to a value determined by the average DC bias, and the capacitance is then determined by charge balance between the gate charge and the depletion charge in the bulk. The relaxation time is extracted by matching the change in inversion capacitance as a function of frequency at very low frequencies since the inversion charge is generated thermally [9].

Following the aggressive scaling of the oxide thickness and the substrate doping levels quantum effects and polysilicon space charge become important for the accurate modeling of the MOS  $C-V$  characteristics. The corresponding device physics is well understood and several engineering models are available [18]–[22]. Most MOSFET models include the polysilicon depletion effects in the inversion and depletion regions of the device operation. However, for varactor modeling the inclusion of the accumulation and (to a lesser extent) inversion region in the polysilicon gate is essential in order to reproduce the fine details of the capacitance variation with the gate drive. For this reason computations performed in the present work include complete expression for the space charge in the gate region, in all regions of operation and not just in depletion. Fig. 3 shows simulation results from our model for an ideal MOS capacitor, with the inclusion of quantum effects only [21], and with poly doping (PD) effects only for both N- and P-gate polysilicon doping. Two levels of gate doping are shown (the doping level is unrealistically low for the N-gate simulations; this is included because it shows that polysilicon inversion is accounted for by our model). Note that polysilicon accumulation “softens” the  $C-V$  dependence near threshold or flatband, depending on the gate doping type. This softening of the transition is observed in devices, and the inclusion of polysilicon accumulation, and not just inversion, improves the overall accuracy of our model fit to data.

#### IV. PARASITIC ELEMENTS

The physical subcircuit of the MOS varactor scalable model is shown embedded in the device cross section in Fig. 1. Overlap

and fringing capacitances are lumped together into  $C_{fr}$ . Parasitic capacitances along the gate length are neglected since the poly is over field or shallow trench oxide and the length is small compared to the width. The fringing capacitance is given by

$$C_{fr} = 2 \cdot C_{frw} \cdot (W_g - D_W) \cdot N_s \cdot N_f \quad (14)$$

where  $C_{frw}$  has units F/m.

The NWELL under the gate oxide forms a parallel combination of bias independent well resistance and a bias dependent accumulation resistance in accumulation. The assumption of bias independent well resistance in depletion follows from the high doping of the surface regions in submicrometer MOSFET technologies. The small NWELL depletion under the oxide is negligible in terms of altering the effective sheet resistance of the NWELL or resulting in significant pinching of the current. The measured results validate this assumption by showing no measurable NWELL resistance variation with voltage in Section V. As the gate bias increases above the flatband condition, an accumulation layer will form. A simple physical model for the accumulation resistance is given by

$$R_{ac} = \frac{\frac{L_g}{2}}{(2 \cdot 3)} \cdot \frac{1}{W_g \cdot \mu_{acV} \cdot Q_{ac} \cdot N_s \cdot N_f} \quad (15)$$

The first divide by 2 is due to the symmetric NWELL contacts bisecting the length. The divide by 3 represents the distributed nature of the resistance. The second divide by 2 is invoked since there are 2 devices in parallel for each gate segment. All additional resistance formulations follow similar arguments, where the length divider will be given by 12. The accumulation charge  $Q_{ac}$  is given by

$$Q_{ac} = C_{ox} \cdot \gamma \sqrt{\Phi_t \left[ \exp\left(-\frac{\psi}{\Phi_t}\right) - 1 \right] + \psi} \quad (16)$$

where the surface potential  $\psi$  follows from Section III. The voltage dependent accumulation mobility is given by

$$\mu_{acV} = \frac{uac}{1 + \theta(V_{FB} - V_{GBi})} \quad (17)$$

where  $uac$  is the bulk mobility,  $\theta$  is the surface scattering parameter, and  $V_{GBi}$  is the internal voltage from the poly to the silicon surface, after the poly resistance and before the nwell resistance. As the internal  $V_{GBi}$  approaches  $V_{FB}$  from negative biases,  $Q_{ac}$  goes to zero and the accumulation resistance approaches an open circuit. Appropriate limiting is applied to  $Q_{ac}$  to avoid a divide by zero in (15).

The bias independent NWELL resistance is given by

$$R_{nwb} = \frac{\rho_{nwell} \cdot \frac{L_g}{12}}{W_g \cdot N_s \cdot N_f} \quad (18)$$

where  $\rho_{nwell}$  is the NWELL sheet resistance under gate oxide.

A significant portion of the MOS varactor resistance is determined by the NWELL end resistance formed by the lightly doped source/drain NWELL contact regions. This resistance does not change with gate length and thus provides the limiting

factor to maximum  $Q$  for minimum  $L_g$ . The end resistance is given by

$$R_{\text{inwe}} = \frac{\rho_{\text{end}}}{2 \cdot W_g \cdot N_s \cdot N_f} \quad (19)$$

where  $\rho_{\text{end}}$  is the unit width end resistance and the divide by 2 represents the symmetric nature of the gate segment. In addition to the lightly doped regions,  $\rho_{\text{end}}$  includes the salicided N<sup>+</sup> and contact resistance.

The poly gate resistance is given by

$$R_{\text{gp}} = \rho_{\text{poly}} \cdot \frac{\left(\frac{W_g}{12}\right)}{L_g \cdot N_s \cdot N_f} + \frac{R_{\text{cnt}}}{(N_s + 1) \cdot N_f} \quad (20)$$

where  $\rho_{\text{poly}}$  is the salicided poly gate sheet resistance and  $R_{\text{cnt}}$  is the metal 1 to silicided poly contact resistance. The silicide to poly contact resistance as described by Litwin [23] and implemented into a MOSFET gate resistance model by Scholten *et al.* [24], is ignored. The gate widths and lengths of typical MOS varactors are large enough to minimize the impact of the silicide to poly contact resistance as demonstrated by the model fits in Section VII. Equation (20) can be easily modified to include this effect for smaller geometries or for technologies with high silicide to poly contact resistance.

To establish the metal 1 resistance and inductance, the length of the metal 1 fingers is given by

$$L_m = W_g \cdot N_s + aagap \cdot (N_s - 1). \quad (21)$$

$R_{\text{gm}}$  and  $R_{\text{sm}}$ , the metal resistances for the gate and NWELL contacts respectively, are given by

$$R_{\text{gm}} = \rho_{m1} \cdot \frac{\frac{L_m}{3}}{W_{m1g} \cdot N_f} \quad (22)$$

$$R_{\text{sm}} = \rho_{m1} \cdot \frac{\frac{L_m}{3}}{W_{m1s} \cdot (N_f + 1)} \quad (23)$$

where  $\rho_{m1}$  is the metal 1 sheet resistance,  $W_{m1g}$  and  $W_{m1s}$  are the widths of the gate and NWELL metal, and  $aagap$  is the break in the active area between segments as shown in Fig. 2. Since there is only contact from one side, the normal factor of 12 is reduced to 3, accounting for the distributed resistance. Using the well known Greenhouse equation for self-inductance, parasitic inductances  $L_{\text{gm}}$  and  $L_{\text{sm}}$ , included respectively for gate and NWELL metal self-inductance, are given by

$$L_{\text{gm}} = \frac{\left(2 \cdot L_m \cdot \left(\log(2 \cdot L_m + t_m) + 0.5 + \frac{(W_{m1g} + t_m)}{3 \cdot L_m}\right)\right)}{N_f} \quad (24)$$

$$L_{\text{sm}} = \frac{\left(2 \cdot L_m \cdot \left(\log(2 \cdot L_m + t_m) + 0.5 + \frac{(W_{m1s} + t_m)}{3 \cdot L_m}\right)\right)}{N_f + 1} \quad (25)$$

where  $t_m$  is the metal 1 thickness [25]. Mutual inductance between these metal paths is ignored in the present work. The

parasitic NWELL-Psub diode  $D_{\text{nw}}$  is added and distributed evenly between the NWELL contacts. Finally  $R_{\text{sub}}$  and  $C_{\text{sub}}$  describe the substrate network elements. More advanced treatments for the NWELL diode distribution and substrate network are not warranted since the NWELL terminal, used for frequency tuning in VCO applications, is an ac ground.

## V. MEASUREMENTS

Test devices are laid out in conventional GSG test pads with related deembedding structures. The GATE is connected to port 1 and NWELL connected to port 2.  $S$ -parameter measurements are performed on an HP8510 network analyzer from 500 MHz to 20 GHz. Prior to extracting model parameters and verifying MOS varactor characteristics, all measurement data is rigorously deembedded. A detailed open-thru deembedding methodology is used in order to properly deembed all pad and feed line related parasitic resistance, capacitance and inductance. The thru deembedding uses an ABCD matrix to extract transmission line related model parameters of the feed lines such as characteristic impedance  $Z_{\text{O-THRU}}$  and propagation constant  $\gamma_{\text{THRU}}$  providing accurate deembedding up to 20 GHz.

The deembedded  $S$ -parameters are converted to  $Y$ -parameters from which the MOS varactor characteristics are extracted. To extract the model parameters, a simple equivalent circuit is used consisting of a series connection of a gate capacitance and a lumped resistance (as opposed to the more precise circuit of Fig. 1). At low frequencies (500 MHz), the total gate capacitance,  $C_{\text{gbi}}$  and  $C_{\text{fr}}$  in Fig. 1, is given by  $\text{imag}(y_{11})/(2\pi f)$ . Varying  $L_g$  (0.5  $\mu\text{m}$  to 5  $\mu\text{m}$ ) at fixed  $W_g = 3 \mu\text{m}$ ,  $N_s = 2$ ,  $N_f = 10$ . Varying  $W_g$  (2  $\mu\text{m}$  to 8  $\mu\text{m}$ ) at fixed  $L_g = 0.5 \mu\text{m}$ ,  $N_s = 2$ ,  $N_f = 10$ . Varying  $N_s$  and  $N_f$  at fixed  $N_s \times N_f = 20$ ,  $L_g = 0.5 \mu\text{m}$  and  $W_g = 3 \mu\text{m}$ . Resistance ( $\text{real}(1/y_{11})$ ) and quality factor ( $Q = \text{imag}(y_{11})/\text{real}(y_{11})$ ) values are extracted in the GHz range where  $\text{real}(y_{11})$  is above the dynamic range of the network analyzer. An important point to note is that since the  $C_{\text{fr}}$  acts to bypass the resistance under the poly, a true measure of the device resistance is not possible by using the lumped technique. Thus it is critical to use the same lumped extraction technique from the simulated and measured  $S$ -parameters. The gate capacitance and lumped resistance extracted from the  $S$ -parameters are used to extract the MOS varactor model parameters as described in the next section.

## VI. MODEL PARAMETER EXTRACTION

The MOS varactor model parameters are physically extracted based on the following set of test devices.

- 1) Varying  $L_g$  (0.5  $\mu\text{m}$  to 5  $\mu\text{m}$ ) at fixed  $W_g = 3 \mu\text{m}$ ,  $N_s = 2$ ,  $N_f = 10$ .
- 2) Varying  $W_g$  (2  $\mu\text{m}$  to 8  $\mu\text{m}$ ) at fixed  $L_g = 0.5 \mu\text{m}$ ,  $N_s = 2$ ,  $N_f = 10$ .
- 3) Varying  $N_s$  and  $N_f$  at fixed  $N_s \times N_f = 20$ ,  $L_g = 0.5 \mu\text{m}$  and  $W_g = 3 \mu\text{m}$ .

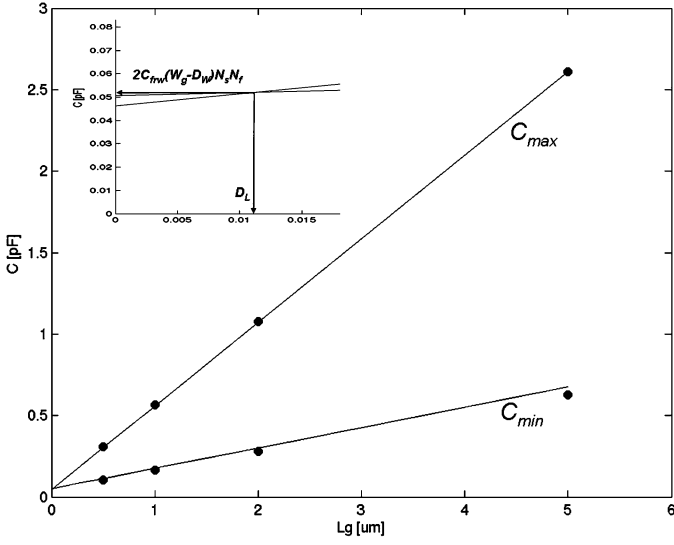


Fig. 4. Measured (solid circles) maximum capacitance ( $V_{GB} = 1$  V) and minimum capacitance ( $V_{GB} = -2$  V) extracted at  $f = 500$  MHz, versus  $L_g$  at  $W_g = 3 \mu\text{m}$ ,  $N_s = 2$ , and  $N_f = 10$ , compared with model extraction (solid line).

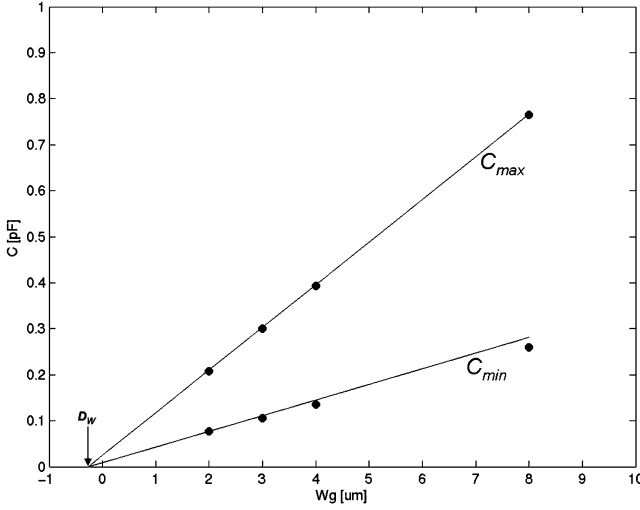


Fig. 5. Measured (solid circles) maximum capacitance ( $V_{GB} = 1$  V) and minimum capacitance ( $V_{GB} = -2$  V) extracted at  $f = 500$  MHz, versus  $W_g$ , compared with model extraction (solid line) at  $L_g = 0.5 \mu\text{m}$ ,  $N_s = 2$ , and  $N_f = 10$ .

The devices are referenced as  $W_g \times L_g \times N_s \times N_f$  throughout the remainder of the discussion.

#### A. Capacitance-Related Model Parameter Extraction

Based on the surface potential MOS charge model described in Section I, the critical model parameters that describe the first order  $C$ - $V$  characteristics are oxide thickness  $T_{ox}$ , flatband voltage  $V_{FB}$  and surface well doping  $N_b$  all of which are closely linked to the process. Since QM effects are included in the charge based model,  $T_{ox}$  represents the physical oxide thickness as opposed to an effective or electrical thickness used in non-QM inclusive models. Additional parameters related to

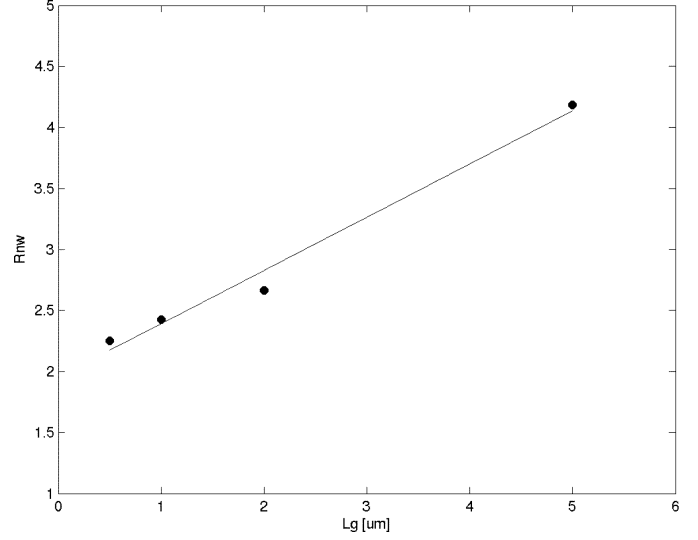


Fig. 6. Measurement extracted NWELL resistance at  $f = 3$  GHz,  $V_{GB} = 0$  V versus  $L_g$ , compared with model extraction (solid line) at  $W_g = 3 \mu\text{m}$ ,  $N_s = 2$ , and  $N_f = 10$ .

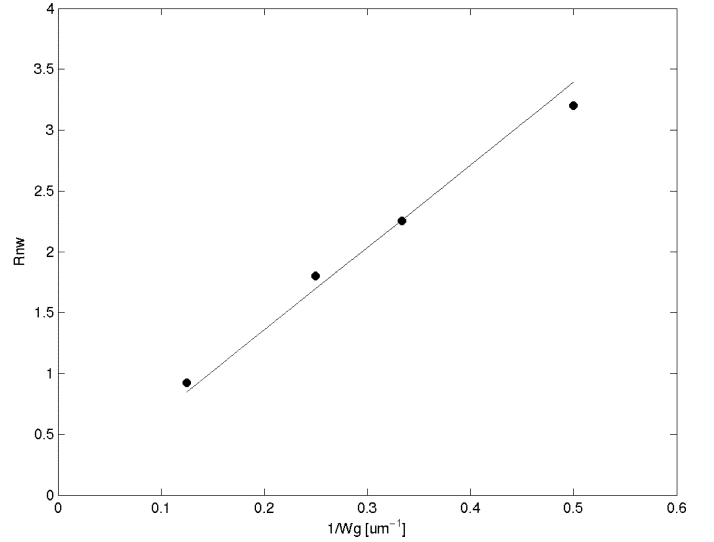


Fig. 7. Measurement extracted NWELL resistance at  $f = 3$  GHz,  $V_{GB} = 0$  V versus  $1/W_g$ , compared with model extraction (solid line) at  $L_g = 0.5 \mu\text{m}$ ,  $N_s = 2$ , and  $N_f = 10$ .

the geometry scaling are  $D_W$ ,  $D_L$ , and  $C_{frw}$ . Simple equations for the maximum and minimum capacitance are given by

$$C_{\max} = (C_{ox} \cdot (L_g - D_L) \cdot (W_g - D_W) + 2C_{frw} \cdot (W_g - D_W)) \cdot (N_s \cdot N_f) \quad (26)$$

$$C_{\min} = \left( \frac{C_{ox} \cdot C_{dep}}{C_{ox} + C_{dep}} \cdot (L_g - D_L) \cdot (W_g - D_W) + 2C_{frw} \cdot (W_g - D_W) \right) \cdot (N_s \cdot N_f). \quad (27)$$

Physically  $D_L$  is the portion of the poly critical dimension (CD) that resides over the NWELL, affecting the nonlinear capacitance with voltage. The rest of the poly CD variation is nondistinguishable from the fringing capacitance and is thus lumped into the  $C_{frw}$  parameter. Note that from  $C_{\max}$  alone it is not possible to independently extract  $D_L$  and  $C_{frw}$ . Introducing

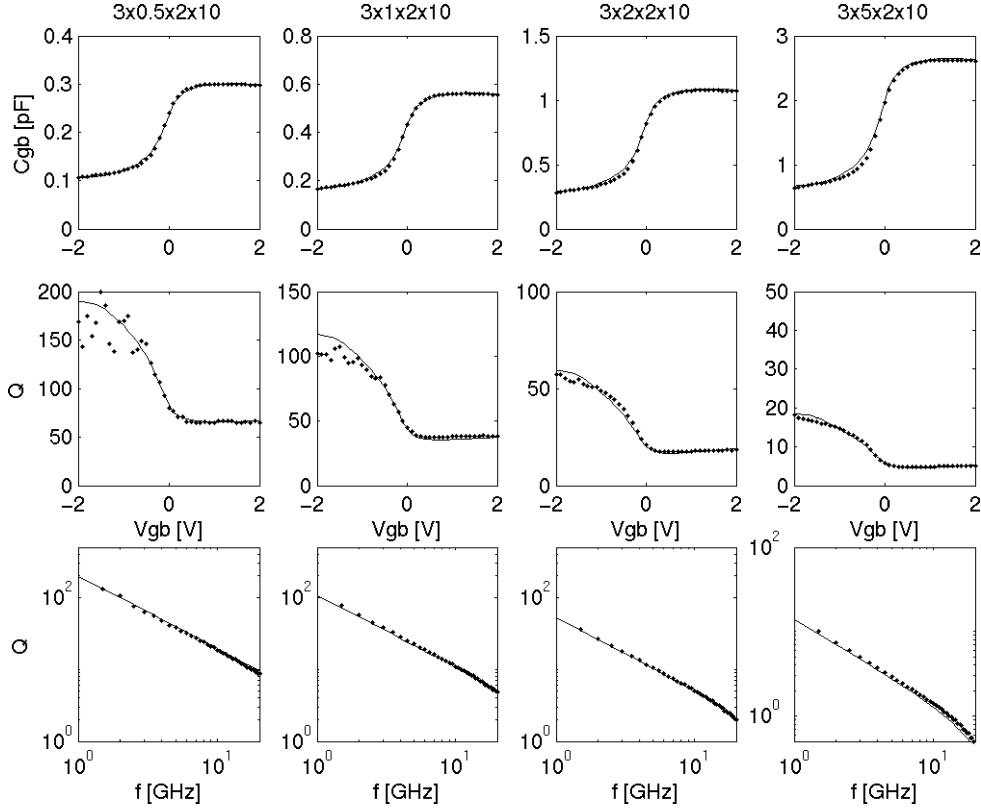


Fig. 8. Measured  $C$ - $V$  (500 MHz),  $Q$ - $V$  (3 GHz), and  $Q$ - $f$ -( $V_{GB} = 1$  V) (solid dots) compared with simulation (solid lines) for varying  $L_g$  at fixed  $W_g = 3 \mu\text{m}$ ,  $N_s = 2$ , and  $N_f = 10$ .

$C_{\min}$  allows the influence of these parameters to be separated. The  $D_W$  is related to the active area CD but will include some parasitic capacitance associated with the *aagap* regions in Fig. 2 not explicitly included in the model. Note that the charge based model produces the  $C_{\text{ox}}$  term in (26) and  $C_{\text{ox}}$  in series with the depletion capacitance  $C_{\text{dep}}$  in (27) thus assuring QM and PD effects are accounted for. Figs. 4 and 5 show  $C_{\max}$  (at  $V_{GB} = 1$  V) and  $C_{\min}$  (at  $V_{GB} = -2$  V) extracted as a function of  $L_g$  and  $W_g$ . The parameter set of  $T_{\text{ox}} = 3.65$  nm,  $D_L = 11.5$  nm,  $D_W = -0.23 \mu\text{m}$ ,  $C_{\text{frw}} = 3.76e - 10$  F/m, is obtained by regression fitting to the data over the  $L_g$  and  $W_g$  space. Regressing  $C_{\max}$  and/or  $C_{\min}$  on  $W_g$ , the abscissa intercept is at  $D_W$ . Regressing  $C_{\max}$  and  $C_{\min}$  on  $L_g$ , the intercept is at the point  $[D_L, (2C_{\text{frw}}(W_g - D_W)N_sN_f)]$ . Extracted values of  $V_{\text{FB}} = 0.6$  and  $N_b = 8.0e17$  provide for the fit to the transition from accumulation into depletion and inversion, shown as part of Figs. 8–10. The model includes the slight poly depletion effects seen near  $V_{GB} = 2$  V.

### B. Resistance-Related Model Parameter Extraction

In order to model MOS varactor  $Q$  characteristics, all resistor-associated components should be physically extracted from test devices with varying  $L_g$  and  $W_g$ . Given the high NWEELL sheet and end resistance compared to metal and poly resistance, the NWEELL resistance dominates the total resistance and hence  $Q$ . The metal resistors  $R_{\text{gm}}$ ,  $R_{\text{sm}}$  and poly-gate resistor  $R_{\text{gp}}$  are directly calculated from (20), (22), (23) with direct input of the process sheet resistance data ( $\rho_{m1} = 66$  m $\Omega$ /sq,  $\rho_{\text{poly}} = 6$   $\Omega$ /sq). To extract NWEELL resistance related parameters, the

measured data at  $V_{GB} = 0$  corresponding to a slight depletion state is used so as to eliminate the effects of accumulation resistance and isolate the NWEELL resistance. The extracted NWEELL resistance is thus given by

$$R_{\text{nwX}} = R_{\text{meas@}V_{GB}=0} - (R_{\text{gm}} + R_{\text{sm}} + R_{\text{gp}}). \quad (28)$$

Equating  $R_{\text{nwX}}$  to the model derived  $R_{\text{nwB}} + R_{\text{nwE}}$ , model parameters  $\rho_{\text{nwell}} = 314$   $\Omega$ /sq and  $\rho_{\text{end}} = 0.24$  m $\Omega \cdot \text{m}$  are directly extracted for test devices with varying  $L_g$  at fixed  $W_g$  using linear regression fitting as shown in Fig. 6. The process monitored  $\rho_{\text{nwell}}$  under thin oxide is 400  $\Omega$ . Thus the extracted value, which is specific to the MOS varactor is in line with the process value. Fig. 7 shows the extracted NWEELL resistance plotted for varying  $1/W_g$  at fixed  $L_g$ . As expected, a linear relationship holds.

## VII. MODEL VALIDATION

After all the capacitance and resistance related parameters are extracted from physical extraction techniques as previously outlined in Section VI, the model is simulated against the entire geometry, voltage and frequency space for  $C$  and  $Q$ , the critical performances for MOS varactor operation. There is no additional optimization steps performed at this point. Figs. 8–10 illustrate the MOS varactor model performance in terms of capacitance and  $Q$  over geometry, voltage, and frequency. Fig. 8 displays simulated and measured data for varying  $L_g$  at fixed  $W_g$ ,  $N_s$ , and  $N_f$ . As  $L_g$  increases, the  $C_{\max}/C_{\min}$  ratio increases due to increased oxide capacitance relative to

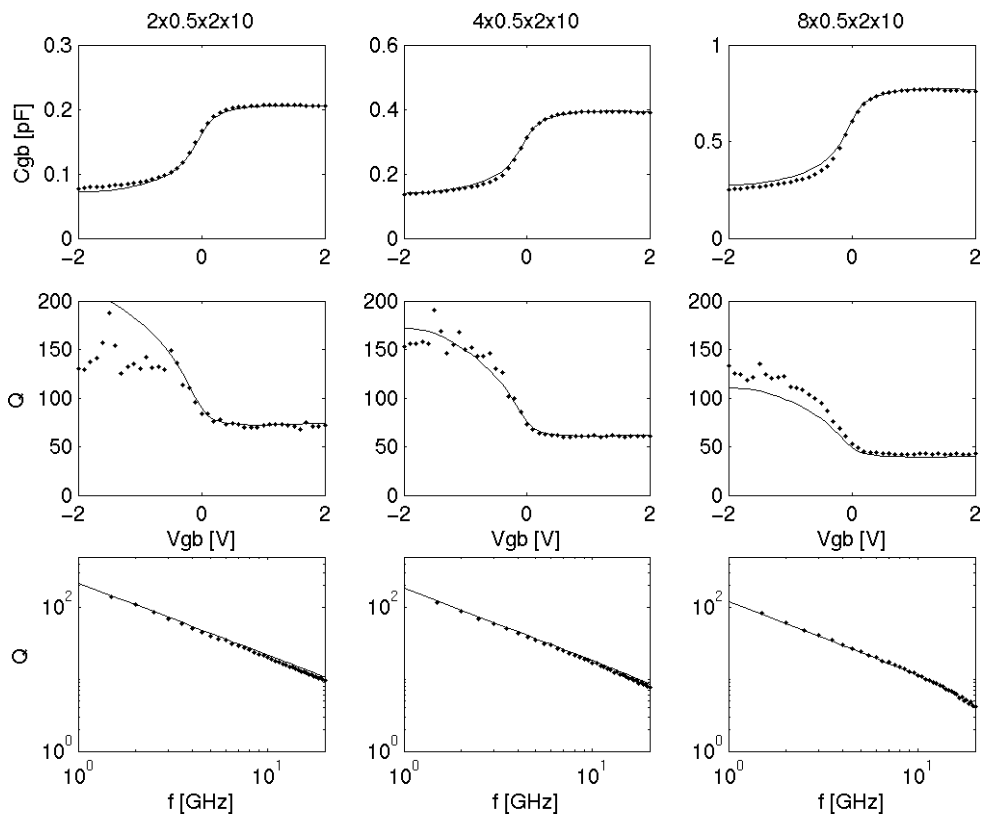


Fig. 9. Measured  $C-V$  (500 MHz),  $Q-V$  (3 GHz), and  $Q-f$ -( $V_{GB} = 1$  V) (solid dots) compared with simulation (solid lines) for varying  $W_g$  at fixed  $L_g = 0.5 \mu\text{m}$ ,  $N_s = 2$ , and  $N_f = 10$ .

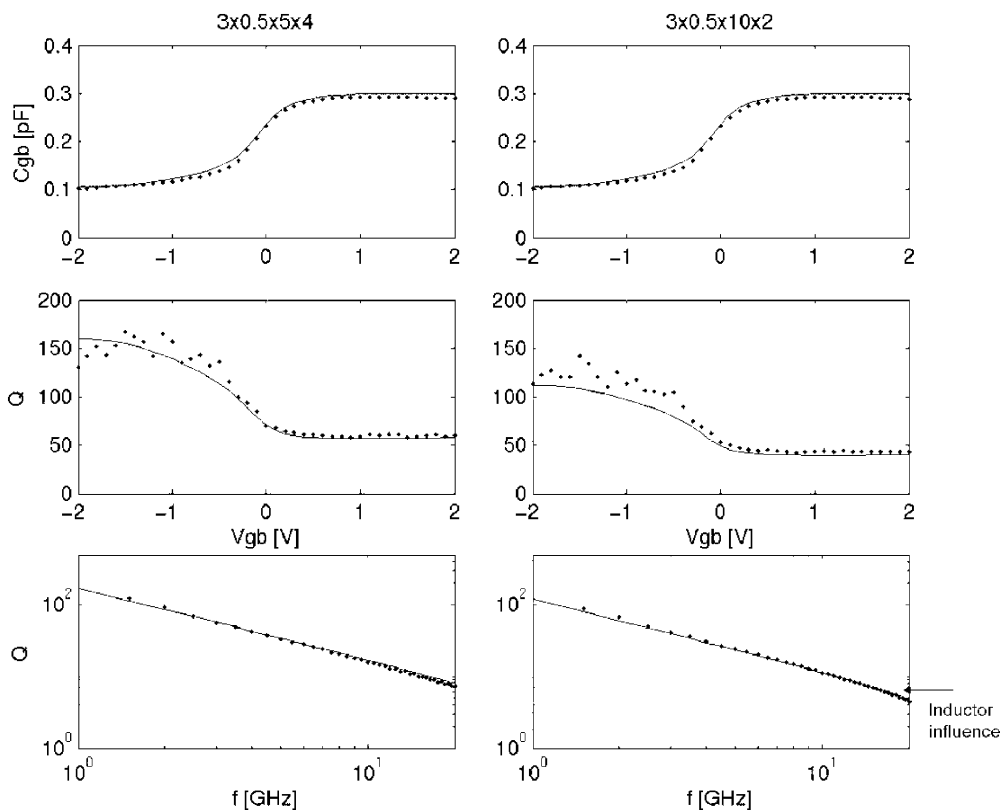


Fig. 10. Measured  $C-V$  (500 MHz),  $Q-V$  (3 GHz), and  $Q-f$ -( $V_{GB} = 1$  V) (solid dots) compared with simulation (solid lines) for varying  $N_s \times N_f$  at fixed  $L_g = 0.5 \mu\text{m}$  and  $W_g = 3 \mu\text{m}$ .

fixed fringing capacitance. The minimum  $Q$  decreases as a result of increasing NWELL resistance with increasing  $L_g$ . Fig. 9 displays simulated and measured data for varying  $W_g$  at fixed  $L_g$ ,  $N_s$ , and  $N_f$ .  $Q$  remains relatively constant up to  $W_g = 4 \mu\text{m}$ . As  $W_g$  increases to  $8 \mu\text{m}$ ,  $Q$  shows a decrease due to higher gate poly resistance. Additionally, the longer finger length resulting from increased  $W_g$  results in inductance affecting the  $Q$ , evident by  $Q$  deviation from the linear trend at frequencies above 10 GHz. Fig. 10 displays simulated and measured data for fixed  $W_g$ ,  $L_g$ , and the  $N_s \times N_f$  product to show the layout dependence of the  $Q$  due to metal interconnect. For  $N_s = 10$ , long metal 1 fingers lead to measurable metal resistance and inductance, degrading the  $Q$  in value by  $\sim 10\%$  (note  $Q_{\min}$  in  $Q-V$ ) and frequency performance (note the rolloff above 10 GHz).

In Section III, physical model equations for the accumulation resistance are presented. However, the  $0.18\text{-}\mu\text{m}$  technology varactors presented in this paper do not exhibit any significant voltage dependent resistance in accumulation proven by the fixed  $Q$  above flatband where the  $C$  is fixed. As the doping underneath the gate is high due to threshold implants (around  $5 \times 10^{17}$ ), any gate voltage induced increase in carrier concentration at the surface is mitigated by reduced mobility due to surface scattering. Thus, the accumulation resistance equations, while physically sound, are more relevant for older technologies where surface doping is reduced.

## VIII. CONCLUSION

A compact scalable MOS varactor model, which for the first time includes an analytical frequency dependent-surface potential based charge model and physical models for all parasitics, was presented. The physical surface potential MOS charge based model includes relevant effects such as QM and poly doping. All parasitic elements including capacitance, resistance and inductance are physically based and scalable. Additionally, the model parameters are heavily process based, thus providing a clear path to statistical and corner modeling. With a robust model parameter extraction methodology, this model has been demonstrated to simulate  $C-V$ ,  $Q-V$  and  $Q-f$  over a wide range of voltage, frequency and geometry space. The proposed model is implemented in Verilog-A to provide portability among various simulators.

## APPENDIX

### ANALYTICAL APPROXIMATION FOR THE MOSFET SURFACE POTENTIAL WITHOUT MINORITY CARRIERS

The normalized form of (11) is

$$(u_g - u)^2 = G^2 [\exp(-u) + u - 1] \quad (\text{A1})$$

where

$$u_g = \frac{(V_{GBI} - V_{FB})}{\Phi_t} \quad (\text{A2})$$

and

$$G = \gamma \Phi_t^{-1/2}. \quad (\text{A3})$$

In what follows

$$\xi = 1 + \frac{G}{\sqrt{2}} \quad (\text{A4})$$

and

$$\sigma(a, c, \tau) = \frac{a(a+c)}{\mu + \mu^{-1}c(a+c)\left(\frac{c^2}{3} - a\right)} \quad (\text{A5})$$

where

$$\mu = \frac{(a+c)^2}{\tau} + \frac{c^2}{2} - a. \quad (\text{A6})$$

For  $u_g \leq 0$  let

$$y_g = -u_g \quad (\text{A7})$$

$$z = \frac{5y_g}{4\xi} \quad (\text{A8})$$

$$\eta = \frac{1}{2}\{z + 10 - [(z-6)^2 + 64]^{1/2}\} \quad (\text{A9})$$

$$a = (y_g - \eta)^2 + G^2(\eta + 1) \quad (\text{A10})$$

$$c = 2(y_g - \eta) - G^2 \quad (\text{A11})$$

$$\tau = -\eta + \log\left(\frac{a}{G^2}\right) \quad (\text{A12})$$

$$y_0 = \eta + \sigma(a, c, \tau) \quad (\text{A13})$$

$$\Delta_0 = \exp(y_0) \quad (\text{A14})$$

$$p = 2(y_g - y_0) + G^2(\Delta_0 - 1) \quad (\text{A15})$$

$$q = (y_g - y_0)^2 + G^2(y_0 - \Delta_0 + 1). \quad (\text{A16})$$

Then

$$u = -y_0 - \frac{2q}{p + \sqrt{p^2 - 2q(2 - G^2\Delta_0)}}. \quad (\text{A17})$$

For  $u_g > 0$  set

$$x_1 = \frac{5}{4} \quad (\text{A18})$$

$$x_{g1} = x_1 + G\sqrt{\exp(-x_1) + x_1 - 1} \quad (\text{A19})$$

$$\bar{x} = \left(\frac{u_g}{\xi}\right) \left[1 + \frac{u_g(\xi x_1 - x_{g1})}{x_{g1}^2}\right] \quad (\text{A20})$$

$$x_0 = u_g + \frac{G^2}{2} - G \left[ u_g + \frac{G^2}{4} - 1 + \exp(-\bar{x}) \right]^{1/2} \quad (\text{A21})$$

$$\Delta_1 = \exp(-x_0) \quad (\text{A22})$$

$$p = 2(u_g - x_0) + G^2(1 - \Delta_1) \quad (\text{A23})$$

$$q = (u_g - x_0)^2 - G^2(x_0 + \Delta_1 - 1) \quad (\text{A24})$$

$$u = x_0 + \frac{2q}{p + \sqrt{p^2 - 2q(2 - G^2\Delta_1)}}. \quad (\text{A25})$$

It may be convenient to use  $u = u_g/\xi$  for  $|u_g| \leq 10^{-7}\xi$  in order to reduce the numerical noise for  $V_{GBI}$  close to  $V_{FB}$ .

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**James Victory** (M'90–SM'01) received the B.S.E.E., M.S.E.E., and Ph.D. degrees in electrical engineering from Arizona State University, Tempe, in 1990, 1992, and 1994 respectively.

In 1992, he joined the semiconductor products sector of Motorola, Inc., Tempe, becoming a Principal Member of Technical Staff, specializing in semiconductor device modeling for circuit simulation of RF analog and power technologies. From 1997 to 2001, he managed the ramp up of an RF semiconductor characterization and modeling lab for Motorola's European IC design center, Geneva, Switzerland. In 2001, he joined ultrawidewand (UWB) startup XtremeSpectrum, where he was Director of Semiconductor Technology and was a key contributor to two generations of UWB chipsets in RFCMOS and SiGe BiCMOS. In 2003, he joined Jazz Semiconductor, Newport Beach, CA, as Manager of the RF characterization and modeling team. He has published over 20 technical journal and conference articles on semiconductor device modeling for power and RF applications.



**Zhixin Yan** (M'81) received the B.S. degree in applied physics from Shanghai University of Science and Technology, Shanghai, China, and the M.S. degree in electrical engineering from Simon Fraser University, Burnaby, BC, Canada, in 1963 and 1992, respectively.

He joined the Department of Applied Physics, Shanghai University of Science and Technology, in 1963, where he taught and performed research on semiconductor devices and integrated circuit design. During 1980 to 1981, he was a Visiting Scholar at Carnegie-Mellon University, Pittsburgh, PA, researching GaAs DLTS. During 1981 to 1982, he was a Visiting Scholar, University of Maryland, College Park, working on VLSI CAD. From 1989 to 1996, he was a Research Associate, School of Engineering Science, Simon Fraser University, working on device modeling and simulation for submicrometer MOSFETs, gated lateral PNPs, and resonant tunnel diodes. From 1996 to 2002, he was an RF device modeling engineer in Rockwell Semiconductor Systems (later Conexant Systems, then Mindspeed Technology). In 2002, he joined Jazz Semiconductor, Newport Beach, CA, as Senior Staff Engineer, working in the area of RF device modeling. His current research interests include RF device modeling for both passive and active semiconductor devices.



**Gennady Gildenblat** (M'83–SM'87) received the M.S.E.E. (with honors) from the (then) Leningrad Electrical Engineering Institute, St. Petersburg, Russia, in 1975, and the Ph.D. degree in solid-state physics from the Rensselaer Polytechnic Institute, Troy, NY, in 1984.

In 1979, he joined the General Electric Corporate and Development Center, Schenectady, NY, where he was engaged in various aspects of the physics and IC technology development. Between 1984 and 1986, he supervised CryoCMOS device engineering study at the Digital Equipment Corporation, Hudson, MA. In 1986, he joined The Pennsylvania State University, University Park, where he presently is a Professor of electrical engineering. His research interests include semiconductor physics and modeling, quantum physics of low-dimensional systems, and semiconductor transport. He has over 100 publications in these areas including several books, invited articles, and U.S. patents.



**Colin McAndrew** (S'82–M'84–SM'90–F'04) received the M.A.Sc. and Ph.D. degrees in systems design engineering from the University of Waterloo, Waterloo, ON, Canada, in 1982 and 1984 respectively, and the B.E. (Hons.) degree in electrical engineering from Monash University, Melbourne, Victoria, Australia, in 1978.

From 1978 to 1980 and from 1984 to 1987, he was with the Herman Research Laboratories of the State Electricity Commission, Victoria. From 1987 to 1995, he was with AT&T Bell Laboratories, Allentown, PA. Since 1995, he has been with Motorola and Freescale Semiconductor, Tempe, AZ, and is at present Director, Enabling Technology. His work is primarily on compact and statistical modeling and characterization for circuit simulation.

Dr. McAndrew is or has been on the technical program committees for the IEEE BCTM, ICMTS, CICC, and BMAS conferences, and is an Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES.



**Jie Zheng** received the B.S. degree from ZheJiang University, the M.S. degree from Union College, Union College, Schenectady, New York, and the Ph.D. degree from Arizona State University, Tempe, in 1982, 1987, and 1991, all in electrical engineering.

He was with Silicon Systems as a Device Model Engineer. Since 1996, he has been with Rockwell Semiconductor Systems, Newport Beach, CA, (now Jazz Semiconductor Inc.) where he is responsible for RF device characterization and device modeling.