

Mixed-signal 0.18 μ m CMOS and SiGe BiCMOS foundry technologies for ROIC applications

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ABSTRACT

Today's readout integrated-circuits (ROICs) require a high level of integration of high performance analog and low power digital logic. TowerJazz offers a commercial 0.18 μ m CMOS technology platform for mixed-signal, RF, and high performance analog applications which can be used for ROIC applications. The commercial CA18HD dual gate oxide 1.8V/3.3V and CA18HA dual gate oxide 1.8V/5V RF/mixed signal processes, consisting of six layers of metallization, have high density stacked linear MIM capacitors, high-value resistors, triple-well isolation and thick top aluminum metal. The CA18HA process also has scalable drain extended LDMOS devices, up to 40V V_{ds} , for high-voltage sensor applications, and high-performance bipolars for low noise requirements in ROICs. Also discussed are the available features of the commercial SBC18 SiGe BiCMOS platform with SiGe NPNs operating up to 200/200GHz (f_T/f_{MAX} frequencies in manufacturing and demonstrated to 270 GHz f_T , for reduced noise and integrated RF capabilities which could be used in ROICs. Implementation of these technologies in a thick film SOI process for integrated RF switch and power management and the availability of high f_T vertical PNPs to enable complementary BiCMOS (CBiCMOS), for RF enabled ROICs, are also described in this paper.

KEYWORDS

ROIC, silicon-germanium, SiGe BiCMOS, MIM capacitor, LDMOS, NPN, PNP, SOI, complementary BiCMOS

1. INTRODUCTION

Read out integrated circuits (ROICs) are used for consumer, industrial, scientific and military needs such as automobile and maritime night vision, surveillance, medical and X-ray imaging, building diagnostics, fire fighting, gas detection, helmet mounted and weapons sights, smart munitions, micro-UAVs (unmanned aerial vehicles), etc. The ROICs are typically hybridized with high performance sensors or have integrated detectors for applications ranging from X-ray to long wave infrared (LWIR) and beyond wavelengths. Thermal imaging applications have been extensively documented and drive most of the wafer volumes in ROICs. As these applications mature, there is an increasing requirement to add more functionality and minimize power consumption for both cooled^{1,2,3,4} and uncooled^{5,6,7} thermal imaging applications. Specialty foundry TowerJazz, driven by high volume commercial needs in the radio frequency (RF), high performance analog, imaging and power markets, offers a high level of integration of active and passive devices in various CMOS nodes. These integrated features include high performance passive devices such as metal-insulator-metal (MIM) capacitors, resistors, thick top metal for inductors, various active devices such as native FETs, NPNs, PNPs, drain extended LDMOS devices, various isolation schemes such as deep trench, SOI, deep N-well and high resistivity substrates, and combinations of features from different CMOS nodes to optimize performance and meet challenging design requirements.⁸ One of these CMOS nodes, the feature rich modular mixed-signal 0.18 μ m CMOS platform could become the technology of choice for next generation ROICs as it could enable migration to lower noise, smaller pixel sizes, lower power consumption, and higher functional integration. The latter includes potential embedded wireless features for RF enabled ROICs, as integrated solutions from DC to mmWave can be achieved in this technology node using silicon germanium (SiGe) BiCMOS process technology.

In this paper, we will focus on the possibilities of integrating process features available in the 0.18 μm platform for future ROIC applications. First, we will detail the CMOS and SiGe BiCMOS process technologies in the 0.18 μm technology node at TowerJazz that could be used for ROICs. Second, we will describe additional process modules available in the 0.18 μm node for commercial applications, such as thick film SOI and complementary BiCMOS, for potential RF enabled ROIC applications.

2. 0.18 μm CMOS AND SiGe BICMOS PROCESS TECHNOLOGIES

In this section, we will describe the dual gate oxide 1.8V/3.3V CA18HD process technology, dual gate oxide 1.8V/5V CA18HA process technology, and the SBC18HA SiGe BiCMOS process technology which have been developed for commercial, mixed signal, analog, RF and power management products and which can be used for future ROICs and RF enabled ROICs.

2.1 CA18HD process technology

The CA18HD process technology supports 1.8V digital CMOS with 26 \AA (physically measured) pure gate oxide and 0.18 μm minimum drawn gate length. The dual gate oxide CA18HD process also has transistors for interfacing to circuits up to 3.3V nominal with 57 \AA (physically measured) thick pure gate oxide. Table 1 summarizes the features of the CA18HD process technology. This digital/mixed-signal/RF CMOS process has six layers of aluminum metallization. The top metallization consists of 2.8 μm thick aluminum metallization with 4.5 μm design rule pitch enabling integration of compact high Q inductors for RF applications and efficient power distribution and low I-R drops across large die. The schematic cross-section of the CA18HD process in Fig. 1 shows the thick top metallization scheme. The TowerJazz CA18 process technology node has highly linear 2fF/ μm^2 density MIM and 4fF/ μm^2 density stacked MIM precision capacitors.⁸ The CA18HD process also supports high value (1kOhm/sq) and low value (310kOhm/sq) unsilicided poly resistors, silicided poly resistors and nwell resistors. The high value unsilicided poly resistors can be used for quenching circuits and resistive trans-impedance amplifiers (RTIA). They also have low mismatch, enabling realization of compact analog circuit blocks. The triple well isolation using deep n-well allows a convenient substrate isolation scheme for individual devices and circuit blocks, in addition to the ability to implement body biasing. This process also has pure gate oxide instead of nitrided gate oxide. Most other foundries, offering equivalent dual gate oxide 1.8V/3.3V processes, have nitrided gate oxides which introduce charge traps thereby resulting in higher low frequency noise versus pure gate oxides. Cryogenic models down to 78K are available for this process variant. Many of these elements for RF and mixed signal commercial applications are also attractive for ROIC designs.

Process		CA18HD	Units	
CMOS	3.3V NMOS	Vt	0.62	V
		I _{dsat}	0.6	mA/ μm
		Gate L	0.36	μm
	3.3V PMOS	Vt	0.74	V
		I _{dsat}	0.25	mA/ μm
		Gate L	0.3	μm
	1.8V NMOS	Vt	0.52	V
		I _{dsat}	0.6	mA/ μm
		Gate L	0.18	μm
	1.8V PMOS	Vt	0.44	V
		I _{dsat}	0.26	mA/ μm
		Gate L	0.18	μm
		Metal 1 pitch	0.46	μm
	Metal layers	6		
Resistor	Nwell	890	ohm/sq	
	Poly (low value)	310	ohm/sq	
	Poly (high value)	1000	ohm/sq	
Capacitor	MIM	2,4	fF/ μm^2	
Native FET		yes		
Triple Well Isolation		yes		
Isolation		STI		

Table 1: Features of CA18HD process technology.

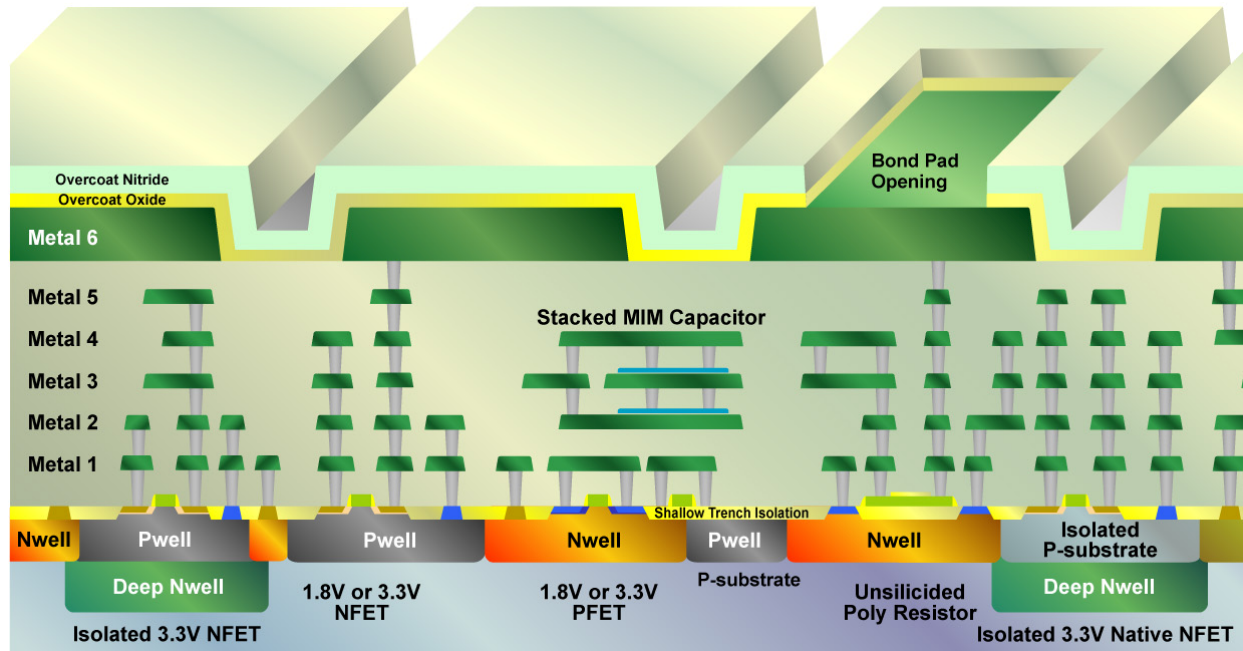


Fig. 1: Schematic cross-section of the 1.8/3.3V CA18HD process technology.

2.2 CA18HA process technology

The CA18HA process is another dual gate oxide 1.8V/5V CMOS process for interfacing to circuits up to 5V nominal with 130Å (physically measured) thick pure gate oxide transistors. In comparison to the CA18HD process described in the earlier section, the CA18HA process has the 3.3V FETs replaced by the 5V FETs, while preserving the other active and passive devices and metallization scheme of the CA18HD process. A summary of the CMOS parameters for the CA18HA process is made in Table 2.

Process		CA18HA	Units	
CMOS	5V NMOS	Vt	0.65	V
		Idsat	0.52	mA/μm
		Gate L	0.6	μm
	5V PMOS	Vt	0.77	V
		Idsat	0.26	mA/μm
		Gate L	0.6	μm
	1.8V NMOS	Vt	0.52	V
		Idsat	0.6	mA/μm
		Gate L	0.18	μm
	1.8V PMOS	Vt	0.44	V
		Idsat	0.26	mA/μm
		Gate L	0.18	μm
	Metal 1 pitch	0.46	μm	
	Metal layers	6		
Resistor	Nwell	890	ohm/sq	
	Poly (low value)	310	ohm/sq	
	Poly (high value)	1000	ohm/sq	
Capacitor	MIM	2,4	fF/μm ²	
Native FET		yes		
Triple Well Isolation		yes		
Isolation		STI		

Table 2: CMOS features for CA18HA process technology platform.

CA18HA						
	Vgs (V)	Vds (V)	Vt (V)	Rdson (mohm-mm ²)	BVDSS (V)	IDSAT (mA/μm)
High Voltage NLDMOS	5	20	0.68	21.5	>25	0.3
	5	40	0.68	50	>45	0.3
Isolated High Voltage NLDMOS	5	20	0.68	27	30	0.3
	5	40	0.68	64	43	0.3
High Voltage PLDMOS	5	20	0.88	79	>25	0.14
	5	40	0.88	169	>45	0.14

CA18HA HV NPN	
Beta	112
Early Voltage	24.5V
Bvceo	>11V
Bvebo	>7V
Bvcbo	>36V

Table 3: LDMOS and NPN features of CA18HA process technology platform.

The schematic cross-section of the CA18HA process is very similar to the CA18HD process in Fig. 1 but with the 3.3V devices being replaced by 5V devices. In addition, the 1.8V/5V CA18HA process has 5V CMOS devices (non-isolated), 5V CMOS devices (isolated with ability to float to > 50V with respect to substrate), 12V drain-extended NFETs (isolated and non-isolated), 12V drain-extended PFETs, 20-40V non-isolated drain-extended NFETs (with breakdown to > 50V), 20-40V isolated drain-extended NFETs, 20-40V drain-extended pFETs and high voltage npn bipolar device (see Table 3).⁹ Power management, low-dropout regulators, display driver, MEMS driver, class D audio amplifier, as well as other advanced applications can be integrated onto the same silicon for commercial needs using these available medium and high voltage drain extended LDMOS devices. These scalable drain-extended devices can also be used for ROICs designed for various high voltage sensor applications and integrated power management. The available bipolar devices can be used for low noise biasing applications as well as in precision band gap voltage reference circuits.

2.3 SBC18HA process technology

With wireless applications becoming pervasive, ROICs will require integrated RF functionality for commercial, scientific and military applications. TowerJazz SiGe BiCMOS processes have found extensive commercial usage from cellular to mmWave applications. In the foreseeable future, it is envisioned that the benefits of the high speed SiGe NPNs will be integrated along with the CMOS features and high performance passives for single chip RF enabled ROIC solutions with low noise, low power and wireless communication capability. So far, we have described the 0.18μm mixed signal CMOS platforms. A 0.18μm SiGe BiCMOS SBC18 process is now described.

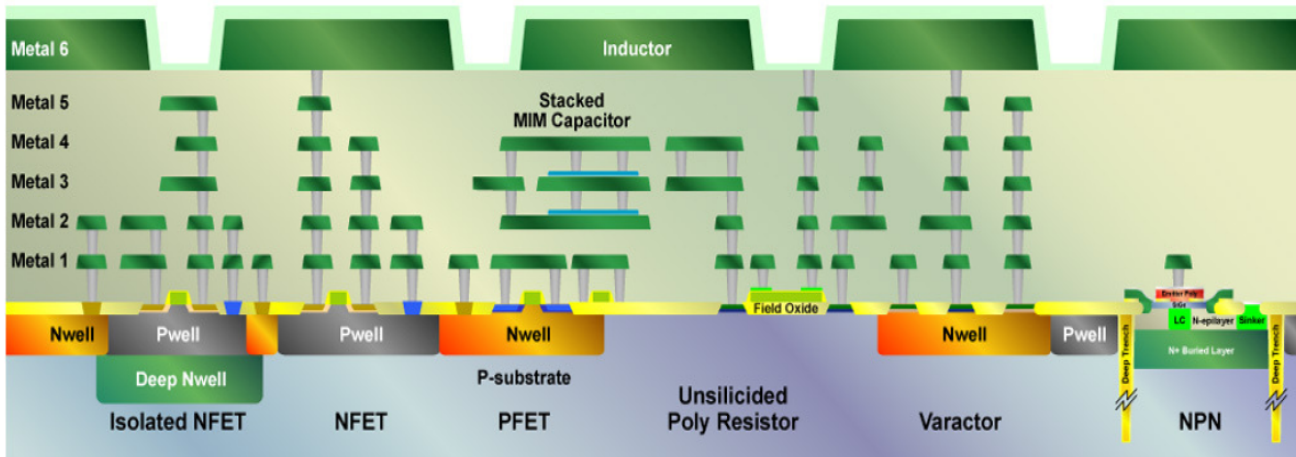


Figure 2: Schematic cross-section of SBC18HA process technology.

Process		SBC18HA	Units	
CMOS	3.3V NMOS	Vt	0.62	V
		I _{dsat}	0.6	mA/μm
		Gate L	0.36	μm
	3.3V PMOS	Vt	0.74	V
		I _{dsat}	0.25	mA/μm
		Gate L	0.3	μm
	1.8V NMOS	Vt	0.52	V
		I _{dsat}	0.6	mA/μm
		Gate L	0.18	μm
	1.8V PMOS	Vt	0.44	V
		I _{dsat}	0.26	mA/μm
		Gate L	0.18	μm
	Metal 1 pitch		0.46	μm
	Metal layers		6	
Resistor	Nwell	890	ohm/sq	
	Poly (low value)	310	ohm/sq	
	Poly (high value)	1000	ohm/sq	
	Metal (low value)	25	ohm/sq	
Capacitor	MIM	2.8, 5.6	fF/μm ²	
Varactor	p+/n Junction	yes		
	Buried Layer Junction	yes		
	MOS	yes		
PNP	Lateral	yes		
	Vertical	yes		
Schottky Diode		yes		
Triple Well Isolation		yes		
Isolation	STI	yes		
	Deep Trench	yes		

(a)

	NPNs in SBC18HA			
	HS	STD	HV	
f _T	150	78	38	GHz
f _{MAX}	190	280	180	GHz
BV _{ceo}	2.2	3.5	6	V

(b)

Table 4: CMOS and NPN features of SBC18HA process technology platform.

The SBC18HA process technology platform integrates NPNs with f_T/f_{MAX} of up to 150/190GHz onto the dual gate 1.8V/3.3V 0.18μm RF/mixed-signal CMOS CA18HD-like process sharing the same CMOS transistors, capacitors and resistors. Fig. 2 shows a schematic of the SBC18 process. Table 4 summarizes the various NPN, CMOS and mixed signal parameters.

The process flow for integration of the modular and scalable NPN device is now described. The SBC18 process flow begins with the formation of the deep n-well and buried layer followed by epi layer deposition. Next, the shallow trench isolation and the deep trench isolation modules are formed. After the NPN collector sinker and the CMOS well formations, the CMOS processing steps of dual gate oxide growth and poly gate patterning and LDD implants are continued up to CMOS spacer deposition. The spacer film stack is removed in the NPN device formation regions and the NPN module is then completed using a self-aligned integration scheme.¹⁰ Separate implant masks are used to change the collector implant profile and obtain the high speed NPN (f_T/f_{MAX} of 150/190GHz) and the standard NPN (f_T/f_{MAX} of 78/280GHz), in addition to the high voltage NPNs (f_T/f_{MAX} of 38/180GHz). The remaining CMOS processing steps are then completed from spacer module onwards after masking the NPNs, including additional masks for buried layer junction varactors, high value resistors, etc. The low threshold native FETs, lateral PNPs, Schottky diodes and MOS varactors, also available in this process, do not require any additional masking steps. The backend of the process has six

metal layers. The top metal layers are 2.8 μm thick metal6 and 1.6 μm thick metal5 aluminum metallization layers connected to each other with 2 μm tall via5. The metal5 is connected to metal4 with a 2 μm tall via4. The remaining metal layers have 0.18 μm node design rule density to facilitate dense routing. The combination of the thick metal layers and thick interlayer dielectrics enable high Q inductors and transmission lines on silicon for RF and mmWave applications as well as use of 0.18 μm CMOS low power and high density digital blocks such as standard cells, IO cells, and memory. The SBC18HA process has the highest density silicon nitride dielectric based 2.8fF/ μm^2 density MIM capacitor and 5.6fF/ μm^2 density stacked MIM capacitors. This process also supports high value (1kOhm/sq) and low value (310kOhm/sq) unsilicided poly resistors, silicided poly resistors and nwell resistors, similar to the CA18HD process. In addition, this process has embedded low-value metal resistors of 25 Ohm/sq for high Q applications. The SBC18 processes also support a lateral PNP. The epi-layer of the NPN transistors forms the intrinsic base of the PNP. The deep N+ sinker and buried layer, common to the NPN, form the extrinsic base. Figure 3 shows the beta versus collector current plot of a 1 μm x 1 μm lateral PNP device.

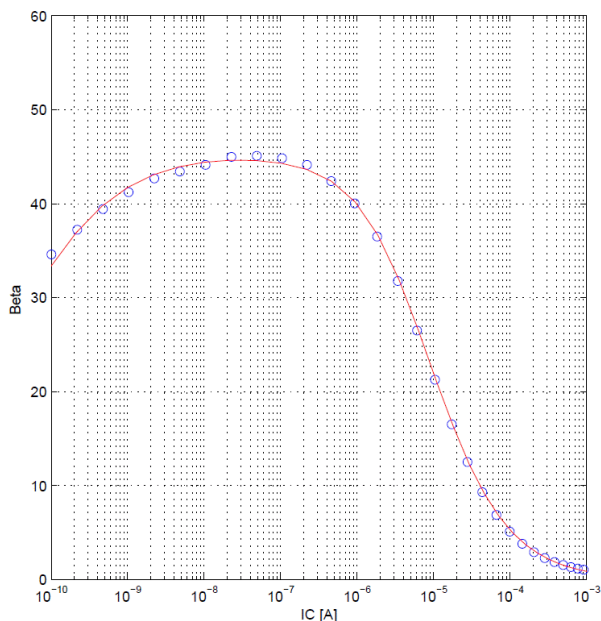


Fig. 3: Beta versus collector current plot of a 1 μm x 1 μm lateral PNP device.

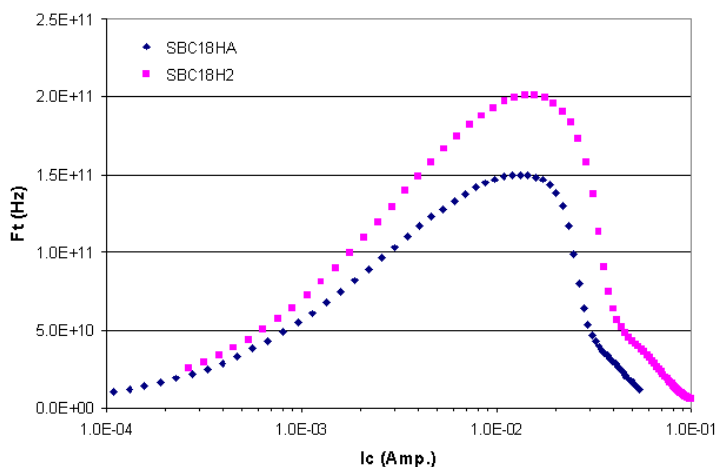


Fig. 4: f_T versus collector current plots for High Speed NPNs in SBC18HA and SBC18H2.

The TowerJazz SiGe BiCMOS SBC18HA process has been used in a variety of applications such as cellular transceivers and power amplifiers, mobile broadband, optical networking, and mmWave applications.^{11, 12} Since this scalable NPN architecture is integrated onto the CA18 mixed-signal CMOS platform without any model changes to the FETs and passives, this enables existing digital and mixed signal blocks built into the CA18HD platform to be reused into the SBC18HA SiGe BiCMOS platform while designing circuit blocks using the bipolar devices. This versatility could enable highly integrated radio-enabled ROIC chips in the future. The scalable NPN architecture has been extended to the SBC18H2 process technology platform with high speed NPN of 200/200GHz f_T/f_{MAX} . Figure 4 shows the f_T versus collector current plots for High Speed NPNs in SBC18HA (150GHz) and SBC18H2 (200GHz). Also, a higher performance NPN with f_T/f_{MAX} of 270/270GHz has been proposed with measured NPNs of $f_T = 270$ GHz integrated into the SBC18 platform.¹³

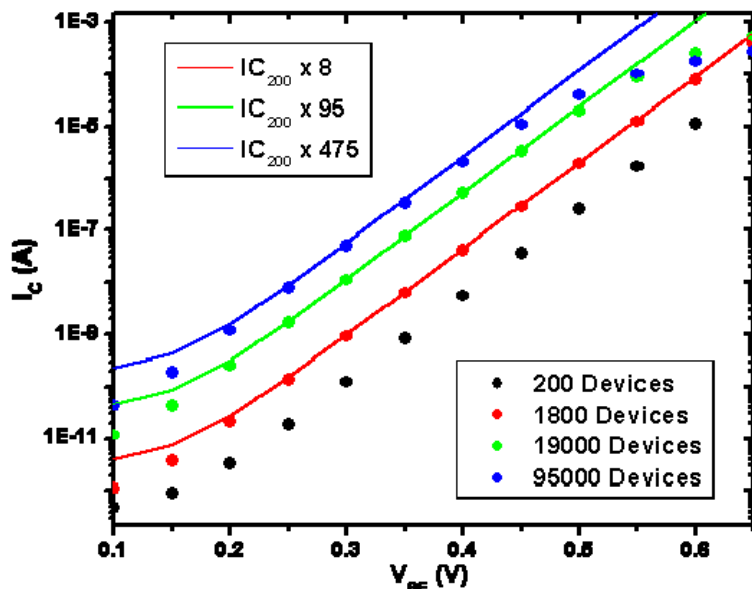


Fig. 5: Collector current vs. V_{BE} measurements across large NPN arrays.¹⁴

Depending upon future integration requirements of these NPNs into ROICs, NPNs greater than few hundred thousand may have to be functional within each die. Typical bipolar or BiCMOS circuits do not exceed more than 1000 NPNs. However, TowerJazz collects NPN yield information from large arrays as is shown in Fig. 5.¹⁴ These arrayed structures are sensitive to I_C shorts and leakages but not opens. An additional scheme for monitoring open devices in large NPN arrays has also been developed. These arrays show excellent I_C scaling and are routinely monitored. A commercial product with more than 700,000 NPNs has been built at TowerJazz.

In addition to potential integrated wireless ROIC applications which can be enabled from low GHz to 60GHz and beyond using SiGe BiCMOS technology, this technology can be used directly for imaging applications. Detectors in the low attenuation 94GHz frequency in the W band imaging has been demonstrated using the SBC18H2 technology.¹² Integrated SiGe detectors can also extend the range of the CMOS visible image sensors into the near infrared spectrum.

3. ADDITIONAL DESIGN AND PROCESS FEATURES IN 0.18UM

In this section, we describe some additional features available for commercial applications at TowerJazz, which could be used for future ROICs for focal plane array and sensing applications. Design environments that allow IC design teams to test, modify and improve the functionality and yield of new products long before the first prototype is manufactured are especially important today for ROIC designs. Some of the design enablement features include design rules for sub-field stitching in large die; statistical, X-sigma, process control monitor (PCM) based models and reliability model tool; and local metal density tool to improve process control margins in large die.^{8,12} Some of the enhanced process features used in commercial RF and mixed signal processes, include high density linear MIM capacitors, low noise FETs,

cryogenic models, and stitching have already been described.⁸ SiGe NPNs tailored for power amplifier (PA) applications along with deep-silicon vias (DSV) for low inductance grounds are also available in SBC18 platform.¹⁵ In this section, we describe the availability of complementary BiCMOS and thick film SOI CMOS in the 0.18 μm process node which have been developed and demonstrated for commercial applications for potential integration of RF front-end modules into ROICs.

3.1 Complementary BiCMOS

In many commercial applications, complementary bipolar (PNP + NPN) technology is advantageous over NPN only counterparts for their ability to significantly reduce the power consumption in high-performance analog circuits and high-speed push-pull amplifiers which drive low impedance loads such as in DSL line drivers, variable gain amplifiers, hard disk drive pre-amplifiers and laser diode drivers.^{16,17} A high performance vertical PNP module has been integrated into the TowerJazz SBC18 SiGe BiCMOS process, while maintaining the same NPN performance.¹⁷ Fig. 6 shows high speed PNP transistors demonstrated into the SBC18 platform. The peak f_T is taken with $V_{CB} = -4\text{V}$ in all cases. The device had an emitter area of $0.8 \times 10\mu\text{m}$. Standard offering in this platform include PNP transistors with f_T of 18GHz and with BV_{CEO} of up to 14V.

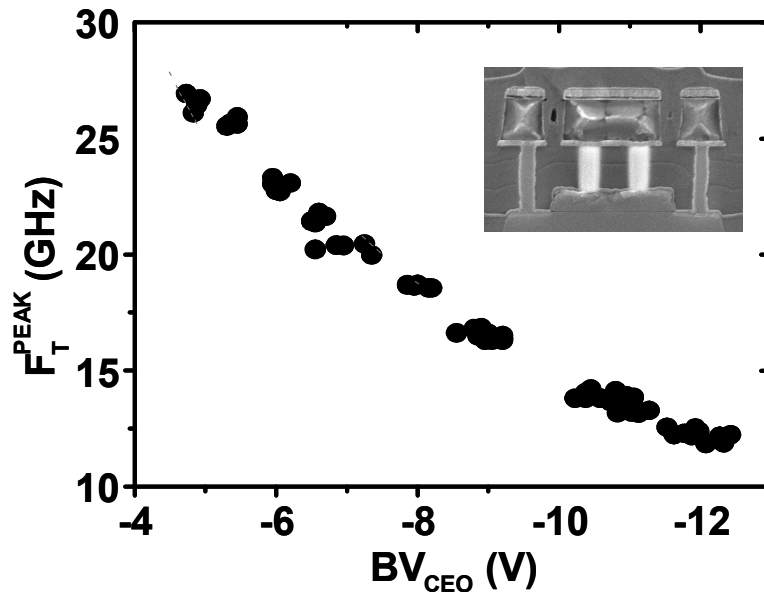


Fig. 6: f_T vs. BV_{CEO} measurements for the TowerJazz PNP transistors in SBC18 technology.¹⁷

3.2 Thick Film SOI CMOS

For cellular PA applications, a thick film SOI CMOS process has been used to integrate RF power amplifier (PA) controllers, high voltage CMOS for power management and RF high power switches for a cost effective die in the 0.5 μm process node.¹⁸ In the 0.18 μm CMOS node, the dual gate oxide 1.8V/3.3V CA18HD and the dual gate oxide 1.8V/5V CA18HA processes have been successfully integrated into the thick film SOI process for the same applications. Figure 7 shows a schematic of the thick film SOI CA18 process. The silicon epi is $> 1\mu\text{m}$ thick. The thick epi allows all the CMOS blocks built in standard bulk wafers, such as PA controllers and power management, to be ported into the SOI process. A deep trench isolation process linking up to the buried oxide layer provides DC and RF isolation between different device wells. The handle wafer is a high resistivity p-type 1000 ohm-cm substrate. This is very useful for RF switch applications, a major component of any RF communication front end module, where a large voltage is isolated by stacking multiple transistors that are allowed to float and distribute the voltage evenly across their terminals. An experimental prototype has also been demonstrated by integrating SiGe BiCMOS SBC18 process on this SOI material. Just like ROICs are built on commercially available mixed signal CMOS processes, enhanced single chip ROIC solutions requiring integrated power management, PAs and RF switches can be built on these SOI CMOS processes.

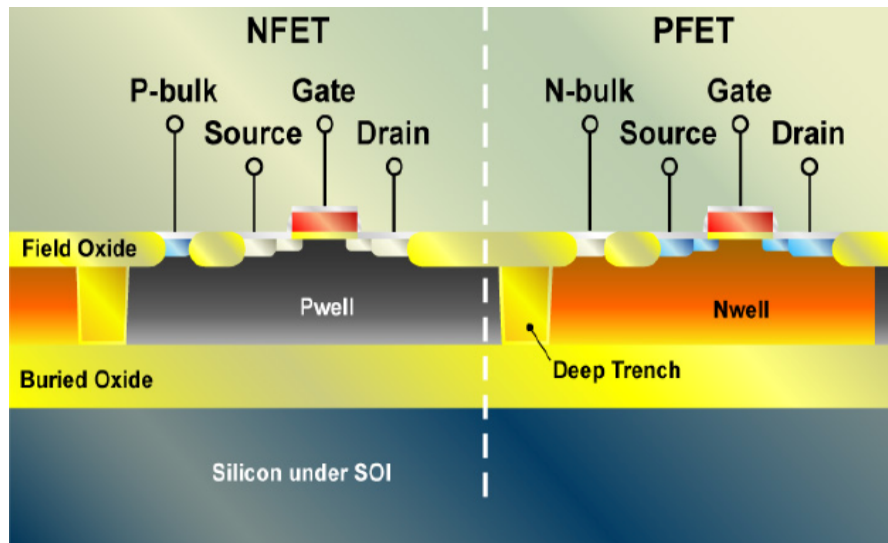


Fig. 7: Schematic of thick film SOI process

4. CONCLUSIONS

In conclusion, the commercial, feature-rich TowerJazz process technology 0.18 μm platforms, such as the CA18HD, CA18HA and SBC18HA, have features that may be highly applicable for use in future ROIC applications. The availability of quality active and passive devices in the dual gate 1.8V/3.3V CA18HD and 1.8V/5V CA18HA commercial processes, such as high density linear stacked 4fF/ μm^2 MIM capacitors, high value and low value poly resistors, low noise NPN bipolars, parasitic vertical PNPs, high voltage LDMOS devices, buried channel pFETs, low threshold voltage native FETs, triple well isolation using deep n-wells for substrate isolation schemes and FET body biasing, and 2.8 μm and thicker metallization across different process platforms were described. The integration of high f_T/f_{MAX} NPNs of up to 150/190GHz in SBC18HA and 200/200GHz in SBC18H2 was also detailed. The SBC18HA process also includes varactors, lateral PNPs, Schottky diodes and low value high-Q metal resistors. Availability of CBiCMOS option and a fully isolated thick film SOI CMOS was also discussed. The additional features enabled using SiGe BiCMOS, CBiCMOS and SOI, which have been used to productize many commercial RF products, is suitable for current and future ROIC needs and potential RF enabled ROIC applications.

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