On-Wafer Inductance and Resistance Characterization of Sub-5pH Deep Silicon Via (DSV)

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***Abstract*—A low parasitic inductance ground for SiGe power amplifiers has been realized using a deep silicon via (DSV). The inductance of the DSV is approximately one order of magnitude smaller than the thru-wafer-via (TWV) inductance of ~21 pH [1] enabling a ground path for power amplifiers in common emitter configuration with literally no parasitic inductance. In this paper we compare two on-wafer measurement approaches, a single port and a two port shunt resonator test structure to characterize such a small inductance. The resistive component in the DSV is dominating and required careful consideration in the two approaches to yield accurate characterization results.**

***Index Terms*—SiGe power amplifiers, common emitter configuration, deep silicon via, thru-wafer via, shunt resonator.**

I. Introduction

The DSV is a tungsten filled plug that connects the lowest interconnect metal layer (M1) to a highly doped p++ silicon substrate. It replaces the ground wire bonds in a common-emitter configuration power amplifier (PA) by providing a path from the transistor emitter to chip lead-frame or PCB by way of the p++ substrate ground plane. Typical applications are in the design of SiGe PA's to ground emitter and shunt elements such as inductors and capacitors as shown with the cross-sections in Fig.1 and Fig.2 [2].

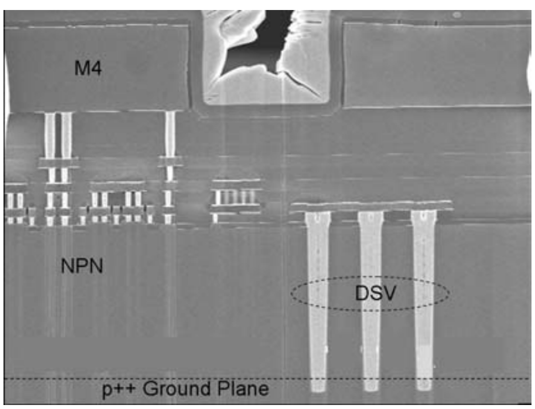

Fig. 1. SBC18 SiGe PA in common emitter configuration with emitter of npn transistors connected to ground using DSV.

A reliable and accurate design process requires scalable models for the DSV that are silicon validated and correctly model the parasitic inductance and resistance of arrays of DSV of variable size. In this work, the inductance of the DSV has been extracted using 2 different on-wafer test approaches and the resistance is obtained from Kelvin DC and single port RF measurements. Owing to the small inductance and large resistance of the DSV, challenges were encountered in the characterization and modeling of the DSV that are described in this paper. In section II, test structure layout and extraction methodology are explained. Measurement and extraction results on single DSV and arrays of DSV are discussed in section III, followed by conclusions in section IV.

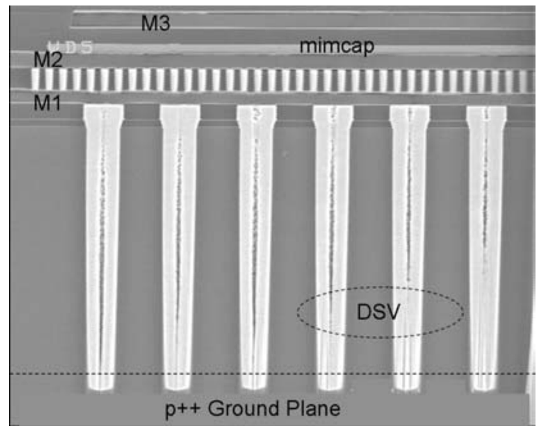

Fig. 2. Shunt Capacitor (Mimcap) with M2 bottom terminal connected to ground using DSV.

II. Test Structure Description and Extraction Methodology

A. DC Resistance Kelvin Test Structure

The DC resistance of the DSV was obtained on a Kelvin test structure as shown in Fig.3. Using the configuration in Fig.3a, the resistance of 2 arrays connected in series by a chain link in the p++ substrate is measured. The result includes resistance contributions from the tungsten plug and, metal to silicon interface and the spreading through the p++ silicon substrate. With the configuration in Fig.3b the resistance of a single array to the wafer backside was measured. The wafer is metalized on the backside to improve contact to wafer chuck or carrier substrate.

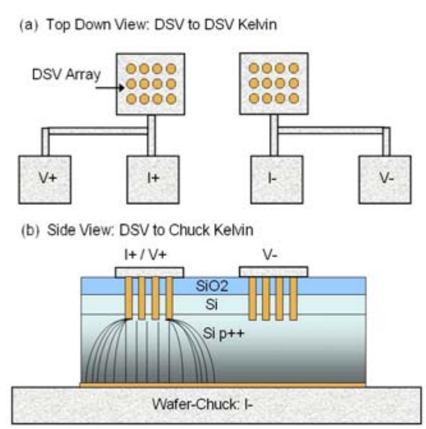

Fig. 3. Schematic view of DC resistance Kelvin test structure

B. RF Measurement 1-Port Test Structure

A single port test structure was used to directly extract resistance and inductance over frequency from the S-parameters. The test structure uses feed lines of various lengths to connect signal probe pad and DSV (Fig.4) [1].

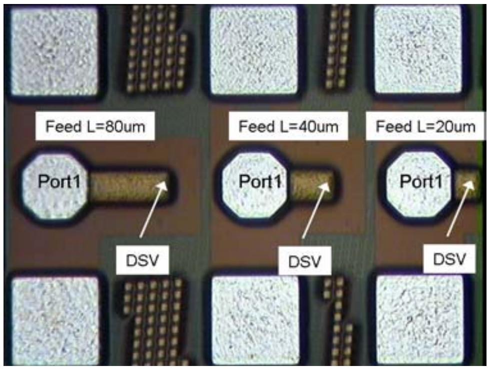

Fig. 4. Single port RF test structure

The resistance and inductance result is extracted from the S-parameters using equations:

$$\boldsymbol{Z}_{11} = \frac{1+\boldsymbol{S}_{11}}{1-\boldsymbol{S}_{11}} \cdot 50 \tag{1}$$

$$\boldsymbol{Ltotal} = \frac{\boldsymbol{imag}(\boldsymbol{Z}_{11})}{2 \cdot \boldsymbol{\pi} \cdot \boldsymbol{f}} \tag{2}$$

$$\boldsymbol{Rtotal} = \boldsymbol{real}(\boldsymbol{Z}_{11}) \tag{3}$$

By extrapolating the measured value over the length of the feed lines, the inductance or resistance of the DSV is obtained from the y-intercept when the length is zero.

C. RF Measurement 2-Port Resonator Test Structure

A two port test structure in T-network configuration was used to indirectly extract inductance from the S-parameters using a shunt resonator approach (Fig.5).

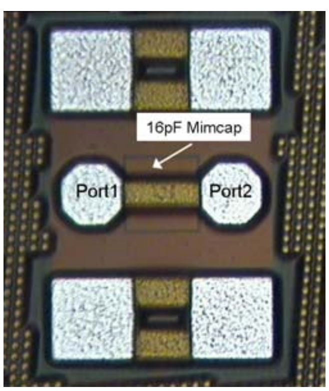

Fig. 5. Two port shunt resonator test structure

This method employs a capacitor that is shunted to ground through the DSV. It also requires a separate test structure to determine the value of the capacitor. The resonance frequency is the frequency at which the phase of Z12 changes sign. Knowing resonance frequency and the capacitance, the inductance value of the DSV is calculated with:

$$\boldsymbol{Lvia} = \frac{1}{(\boldsymbol{f}_{res} \cdot 2 \cdot \boldsymbol{\pi})^2 \cdot \boldsymbol{C}} \tag{4}$$

Due to the expected small value of inductance of less than 5pH a large capacitor is required for resonance within a measurement range of 50 GHz. The calculated resonance frequency with a 16 pF capacitor is 40 GHz and with a 30 pF capacitor is 29 GHz. The PNA network analyzer was calibrated using Line-Reflect-Reflect-Match (LRRM) for a measurement range from 100 MHz to 50 GHz to ensure that the resonance of the shunt resonator is safely captured.

III. Resistance and Inductance Measurement Results

A. Resistance Measurement on Kelvin Structure

The median resistance value (T50) for a single DSV as measured on the Kelvin test structure is 51 Ω (Fig.6).

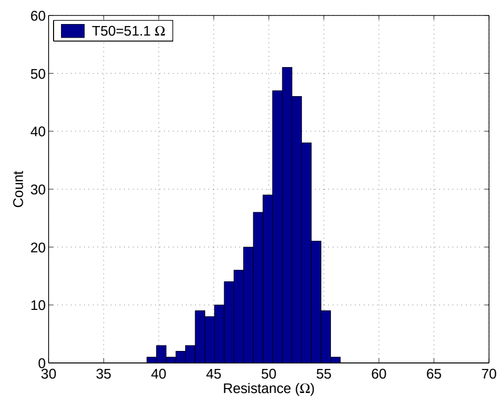

Fig. 6. DC Resistance of single DSV

Using an analytic formulation that assumes a round contact on a semiconducting slab [3], a spreading resistance between 41 to 82 Ω is computed with the lower and upper specification limits of the p++ substrate resistivity. The resistance value of the DSV hence is dominated by the spreading resistance through the p++ substrate, while resistance contributions from tungsten plug and metal to silicon interface are much smaller. Clearly, to obtain a small resistance parasitic on the order of 50 mΩ or less in the emitter ground path of power amplifiers, large distributed arrays of DSV need to be used; and the layout has to be carefully designed to minimize the spreading resistance effect [2].

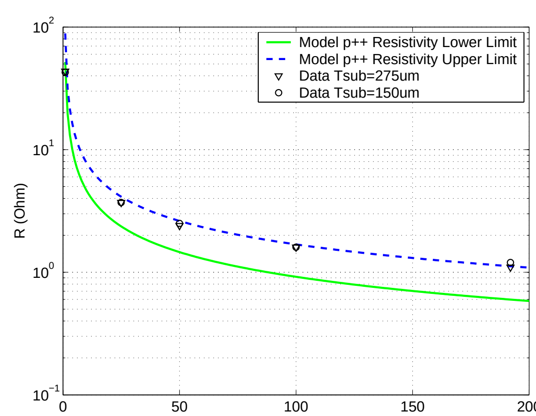

Fig. 7. DC Resistance for DSV arrays of various size

The resistance from top metal to the wafer backside for various size arrays with 1 to 200 DSV was measured on 150 and 275 µm thick wafers after backside grinding and compared to the analytical model (Fig.7). Excellent agreement is achieved, confirming the validity of the spreading resistance model. Furthermore, the spreading resistance is a very weak function of the substrate thickness as shown with the measured data and which is also predicted by the spreading resistance model. The possibility of using thicker substrates rather than requiring the wafer to be thinned to 100 µm offers significant cost and manufacturing benefits.

B. Resistance and Inductance Measurement on 1-Port RF Test Structure

The resistance over frequency for an array of 81 DSV was extracted from the measured S-parameters on the 1-port RF test structure (Fig.8). There is no RF dependence of the resistance expected since the diameter of the DSV is less than the skin depth. Any frequency dependence is due to the metal routing in the test structure. Similar to the Kelvin DC result, the spreading resistance affects results strongly. The extracted DC resistance for the DSV array with the shortest feed length of 20 µm is 2.1 Ω, which agrees closely with the model result of 1.9 Ω.

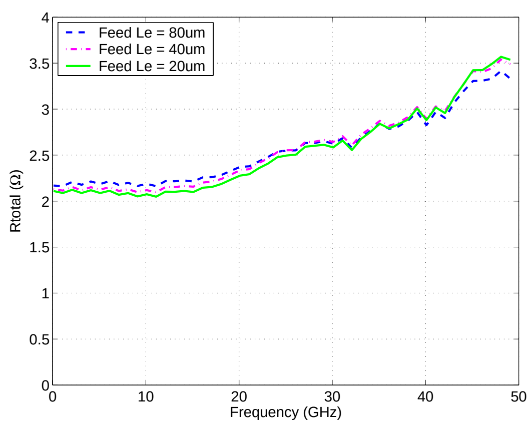

Fig. 8. Resistance over frequency for array of 81 DSV

The inductance of a single DSV is calculated with equation (5) [4] for inductance of a cylindrical hole to 4.2 pH, where h is the depth and r the radius of the DSV:

$$\boldsymbol{L} = 2\cdot\left[\boldsymbol{h}\cdot\ln\left(\frac{\boldsymbol{h}+\sqrt{\boldsymbol{r}^2+\boldsymbol{h}^2}}{\boldsymbol{r}}\right)+\frac{3}{2}\cdot\left(\boldsymbol{r}-\sqrt{\boldsymbol{r}^2+\boldsymbol{h}^2}\right)\right]\cdot 1\boldsymbol{e}-13 \qquad (5)$$

Within an array of DSV, the inductive coupling between individual via needs to be accounted for to accurately model the parasitic inductance of the entire array. Since the shunt current is flowing in the same direction in all DSV towards the p++ ground plane, the mutual inductance will be positive, effectively posing a lower limit of ~0.2 pH for the array regardless of the number of DSV as shown with the simulation results in Fig.9.

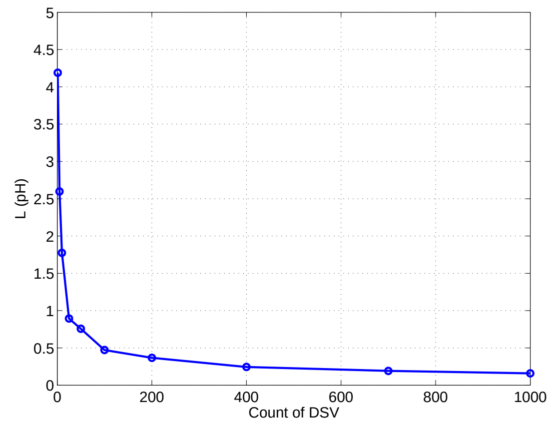

Fig. 9. Simulated inductance for DSV arrays of various size

The inductance of a single DSV was extrapolated from the 1-port test structure measurements to ~2.5 pH, which is in close agreement with the model value of 4.2 pH (Fig.10).

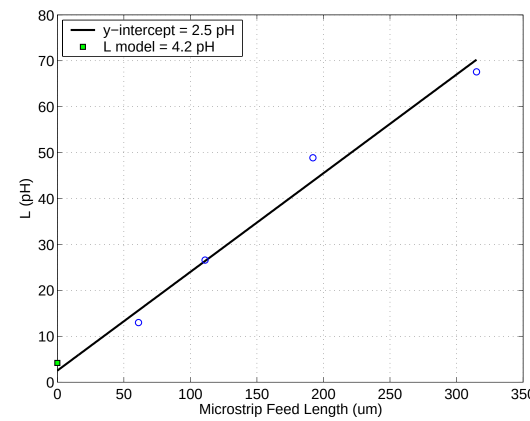

Fig. 10. Inductance of single DSV

In Fig.11, the inductance over frequency for an array of 81 DSV with varying microstrip feed length is shown. As expected, no frequency dependence is observed.

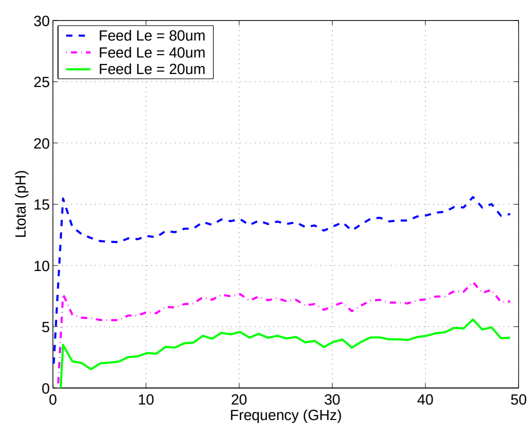

Fig. 11. Inductance over frequency for array of 81 DSV

A general problem was encountered with inductance values being negative at lower frequencies, particular for smaller DSV arrays, requiring in some extractions to use higher frequency points. The authors believe that the spreading resistance and test structure parasitic caused the inductance result to turn negative, which was also confirmed with simulations of the test structure in ADS.

C. Inductance Measurement on 2-Port RF Test Structure

The measured resonance frequency on the shunt resonator test structure with 81 DSV and a capacitor of 16 pF and 30 pF was 28.6 GHz and 22.1 GHz, respectively (Fig.12).

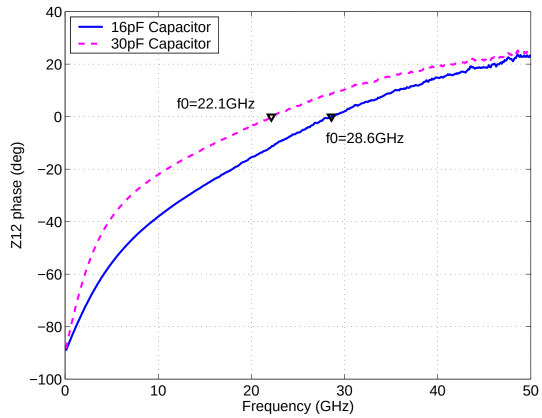

Fig. 12. Z12 Phase of shunt resonator with 81 DSV and 16 pF or 30 pF capacitor

The corresponding inductance values calculated with equation (4) are 2.0 pH and 1.8 pH which agree fairly well with the model value of 0.6 pH considering the small quantities that are being extracted. This method did not have the problem of negative inductance values as observed with the direct extraction method, but rather lacked the expected dip of the S12 transmission coefficient at resonance. The plots of capacitance and S12 for the 16 pF / 2.0 pH shunt resonator show a flat gradient at resonance (Fig.13, 14).

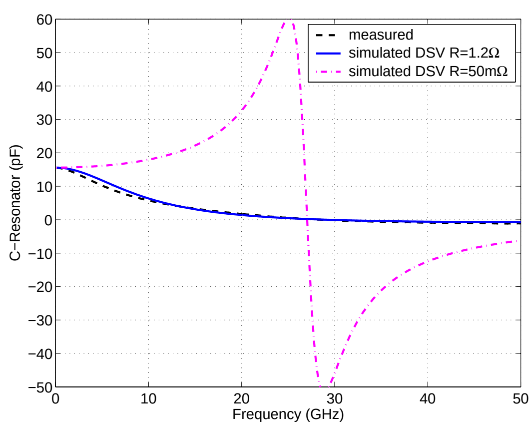

Fig. 13. Capacitance of 16 pF / 2.0 pH (81 DSV) shunt resonator

The measured curves were fit in ADS using an equivalent circuit for the test structure consisting of the shunt resonator with the addition of a parallel capacitance and resistance accounting for the test structure parasitic. A good curve fit was obtained with a resistance of 1.2 Ω for the DSV array and with values from an optimizer for the test structure parasitic. The DSV resistance is smaller than the 2.1 Ω extracted from the 1-port test structure which is likely due to the difference in the structure layout and return current path. After matching the measured curve, the resistance of the DSV was reduced to 50 mΩ and a typical resonance dip was observed, confirming that the spreading resistance value of the DSV array caused the unexpected curve characteristics. The inductance results of the DSV and TWV for reference are summarized in table I.

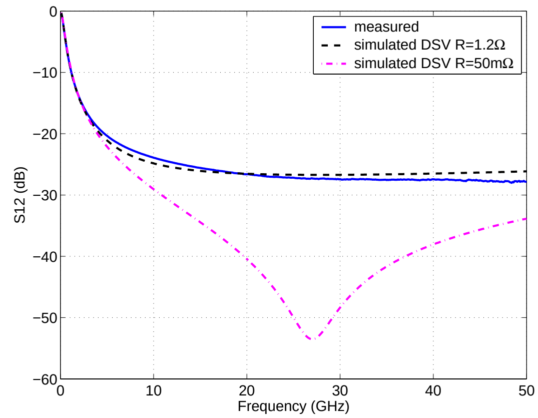

Fig. 14. S21 of 16 pF / 2.0 pH (81 DSV) shunt resonator

TABLE I. INDUCTANCE RESULTS

Ground Method	Measurement Approach	Inductance
1 DSV	Direct (Single Port)	2.5 pH
81 DSV	Shunt Resonator	1.8-2.0 pH
TWV [1]	Shunt Resonator	21.3 pH

IV. CONCLUSION

The deep silicon via (DSV) was shown to have an inductance that is 1 order of magnitude smaller than the TWV permitting shunt connections in a circuit design with literally no parasitic inductance. The parasitic is purely resistive, mainly caused by the spreading resistance through the p++ substrate, dictating the use of large arrays of DSV. This resistance is a weak function of the substrate thickness, eliminating the need for ultra-thin 100 µm substrates as is required for the TWV, offering improved manufacturability and cost benefits.

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