

A Q -Band Four-Element Phased-Array Front-End Receiver With Integrated Wilkinson Power Combiners in $0.18\text{-}\mu\text{m}$ SiGe BiCMOS Technology

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Abstract—A four-element phased-array front-end receiver based on 4-bit RF phase shifters is demonstrated in a standard $0.18\text{-}\mu\text{m}$ SiGe BiCMOS technology for Q -band (30–50 GHz) satellite communications and radar applications. The phased-array receiver uses a corporate-feed approach with on-chip Wilkinson power combiners, and shows a power gain of 10.4 dB with an IIP_3 of -13.8 dBm per element at 38.5 GHz and a 3-dB gain bandwidth of 32.8–44 GHz. The rms gain and phase errors are ≤ 1.2 dB and $\leq 8.7^\circ$ for all 4-bit phase states at 30–50 GHz. The beamformer also results in ≤ 0.4 dB of rms gain mismatch and $\leq 2^\circ$ of rms phase mismatch between the four channels. The channel-to-channel isolation is better than -35 dB at 30–50 GHz. The chip consumes 118 mA from a 5-V supply voltage and overall chip size is $1.4 \times 1.7 \text{ mm}^2$ including all pads and CMOS control electronics.

Index Terms—BiCMOS analog integrated circuit, millimeter wave, multiple input/multiple output (MIMO), phased array, phase shifter, radar, SiGe BiCMOS, smart antenna, Wilkinson coupler, wireless communication.

I. INTRODUCTION

PHASED ARRAYS are very attractive for millimeter-wave (>30 GHz) wireless communications as they can boost the signal-to-noise ratio (SNR); hence, increasing the channel capacity under unfavorable propagation conditions such as atmospheric attenuation and rain fade [1], [2].

In integrated phased-array implementations, the design of a small-sized RF phase shifter with low loss and wide operation bandwidth is a challenging issue, and is one of the main reasons for the alternative approaches of local oscillator (LO) or IF phase-shifting methods [3]–[5]. However, [6] and [7] suggest an active way of multibit phase generation by adding in-phase/quadrature (I/Q) vector signals with proper amplitude controls, and [8] demonstrates a successful realization of miniature 4-bit RF phase shifters based on the active phase interpolation technique at 6–26 GHz in a $0.13\text{-}\mu\text{m}$ CMOS technology. These RF phase shifters were used in the development of an eight-element

phased-array receiver at X - and Ku -band in a $0.18\text{-}\mu\text{m}$ SiGe BiCMOS technology [9]. One of the merits of the RF phased arrays over the IF or LO phase-shifting architectures is that the RF phased arrays can substantially reject an interferer from different directions before being sent to the successive receiver units such as mixers and baseband circuitry, thus maximizing the value of phased arrays as a spatial filter.

This study demonstrates a Q -band (30–50 GHz) four-element phased-array front-end with an *all-RF* architecture where phase shifting and signal combining are done at the RF level [10]. The chip can be used as a standalone chip or as a sub-array for large phased arrays. Specifically, the frequency band in this demonstration is optimized for the satellite systems operating at 36–46 GHz for high data-rate communications, or for defense applications such as high-resolution radars [11]. The phased-array receiver uses on-chip Wilkinson couplers for the RF combiner and this results in excellent performance, as shown in Section V.

II. PHASED-ARRAY ARCHITECTURE

Fig. 1 presents the block diagram of the Q -band phased-array receiver. External filters and HEMT low-noise amplifiers (LNAs) (GaAs or InP, $\text{NF} = 1.5 - 2$ dB and power gain = $10 - 16$ dB @ 40 GHz) precede the silicon beamforming network and the LNA sets the overall system noise figure (NF). This study is focused on the four-element silicon beamforming network, and a single channel is composed of an active balun and a 4-bit RF active phase shifter. The active balun provides broadband impedance matching (50Ω) for the external LNA and wideband single-to-differential signal conversion for the differential phase shifter. The RF active phase shifter is realized using a signal interpolation technique where quadrature signals are added with appropriate amplitudes to obtain the required phase [8]. The output stage of the phase shifter is a differential-to-single (DTS) signal conversion stage and drives the Wilkinson power-combining networks with a $50\text{-}\Omega$ impedance.

In most phased arrays, the power-combining networks should be able to handle large signal levels, requiring good linearity. Wilkinson couplers are excellent candidates in terms of power-handling capability and are integrated compactly in a meandering fashion. The Wilkinson combiners are cascaded in a corporate-feed fashion and provide an easy way of phase calibration at the sub-array level. The phase of each phase shifter can be set independently using a 4-bit digital data input, and a digital array decoder is used to access each phase shifter.

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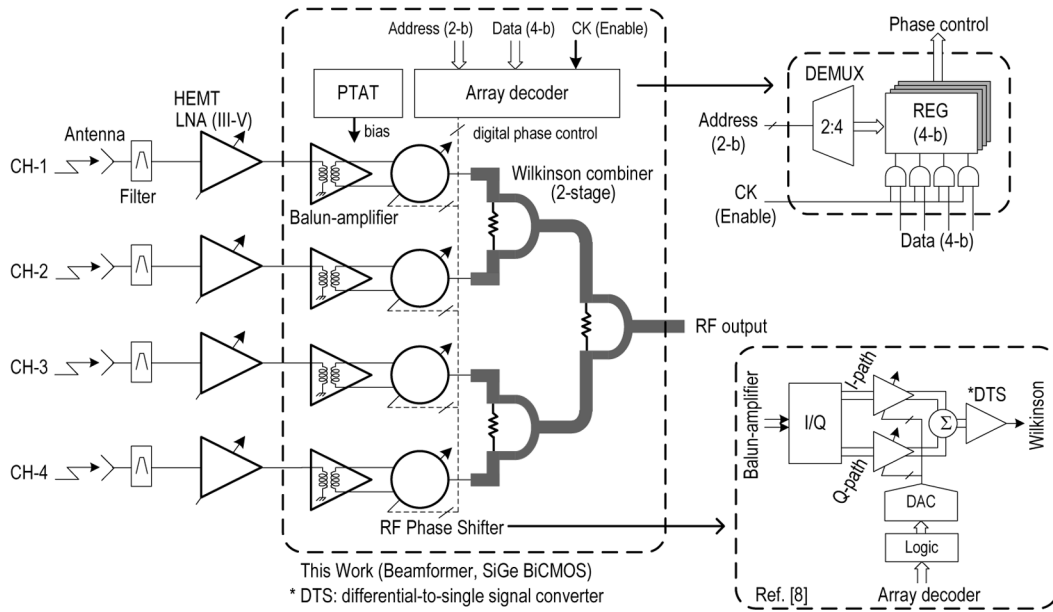


Fig. 1. Functional block diagram of the Q-band phased-array front-end. This study concentrates on the design of the silicon beamforming network.

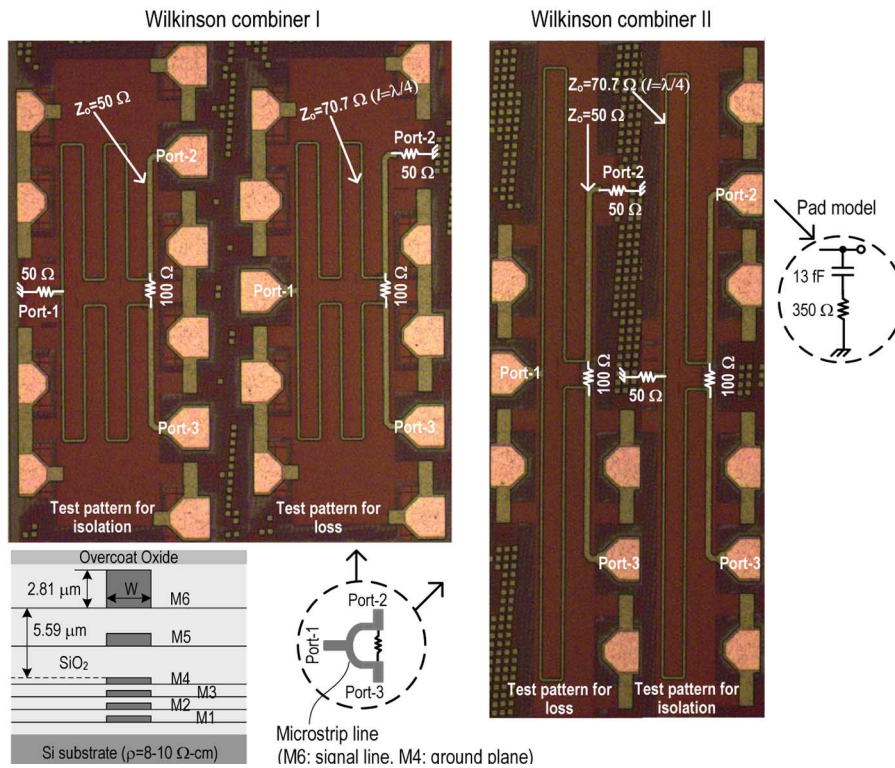


Fig. 2. Test patterns of the integrated Wilkinson power combiners and metal stacks of Jazz SiGe120 process (1P6M). The core areas without pads are $153 \mu\text{m} \times 494 \mu\text{m}$ for the Wilkinson combiner I and $80 \mu\text{m} \times 998 \mu\text{m}$ for the Wilkinson combiner II, respectively.

The array decoder is composed of 4-bit registers ($\times 4$) for memory and 2-to-4 address decoder (DEMUX) for allocating an address to each register [9]. The 4-bit data input is loaded to a register by a corresponding DEMUX output and by an enabling clock signal, and finally uploaded to the logic encoder of the phase shifter having the same address. The logic encoder synthesizes control logic for a digital-to-analog converter (DAC) to change the gains in each of the I- and Q-paths of the phase shifter so as to obtain the 4-bit phase response.

III. INTEGRATED WILKINSON COUPLERS

Fig. 2 presents two different Wilkinson coupler topologies, and the corresponding test patterns for isolation and insertion loss. The Wilkinson combiners are implemented in a standard $0.18\text{-}\mu\text{m}$ SiGe BiCMOS process (Jazz SiGe120, 1P6M) and the corresponding metal stacks are also shown in Fig. 2. The top metal (M6, thickness = $2.81 \mu\text{m}$ and sheet resistance = $10.5 \text{ m}\Omega/\square$) is used for the signal line and

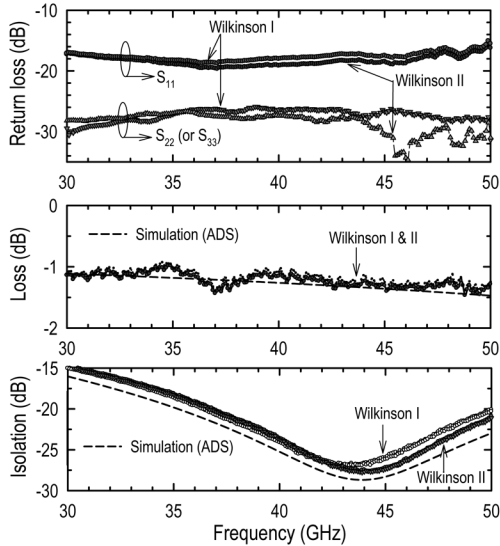


Fig. 3. Measured S -parameters of the Wilkinson combiners. The simulations and measurements include the ground–signal–ground (GSG) pad parasitics.

the ground plane is implemented with M4 (thickness = $0.62 \mu\text{m}$ and sheet resistance = $66 \text{ m}\Omega/\square$). The layouts keep perfect symmetry, and the core sizes excluding pads are $153 \times 494 \mu\text{m}^2$ and $80 \times 998 \mu\text{m}^2$ for the Wilkinson combiner I and II, respectively. For both designs, the port impedance is 50Ω , resulting in a characteristic impedance of 70.7Ω for the quarter-wavelength sections ($l = \lambda/4 = 1045 \mu\text{m}$, $W = 4.06 \mu\text{m}$ @ 44 GHz , SiO_2 $\epsilon_r = 4.2$). The isolation resistor of 100Ω is realized with a TiN metal resistor having a statistical variation of $\pm 14\%$ for 3σ corner models (sheet resistance = $24.5 \Omega/\square$). The output of each port is routed to the pads using a $50\text{-}\Omega$ transmission line ($W = 9.22 \mu\text{m}$).

Fig. 3 shows the measured and simulated (using Agilent Technologies' ADS) S -parameters of the Wilkinson couplers. For both designs, the measured S_{11} is $< -15 \text{ dB}$ and S_{22} (and S_{33}) is $< -26 \text{ dB}$ at $30\text{--}50 \text{ GHz}$. The intrinsic transmission loss, which is S_{13} (or S_{31}) subtracted by -3 dB , is $1\text{--}1.4 \text{ dB}$ at $30\text{--}50 \text{ GHz}$ and matches well with simulations. The results include the transition loss from the pad parasitics, which can be modeled as a shunt capacitor ($C = 13 \text{ fF}$) in series with a resistor ($R = 350 \Omega$). The pad model is estimated based on the library model given by the process foundry. The estimated transition loss in ADS is $0.25\text{--}0.4 \text{ dB}$ per pad at $30\text{--}50 \text{ GHz}$. Therefore, the expected loss between port 1 and port 2 (or port 3) inside the phased-array chip is approximately $0.5\text{--}0.6 \text{ dB}$ per Wilkinson stage at Q -band. The isolation (S_{23} or S_{32}) between ports 2 and 3 is $< -15 \text{ dB}$ at $30\text{--}50 \text{ GHz}$ and $< -20 \text{ dB}$ at $36.8\text{--}50 \text{ GHz}$ for both designs, and matches well with ADS simulations.

IV. ACTIVE CIRCUIT DESIGN

A. Balun Amplifier

Fig. 4 presents the balun amplifier. The first common-base stage provides broadband $50\text{-}\Omega$ match for the preceding external LNA. The balun function is realized in the second stage

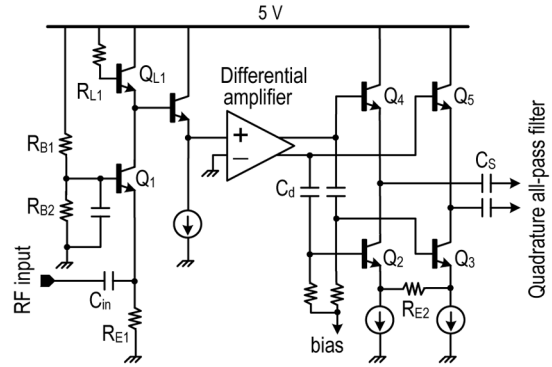


Fig. 4. Q -band balun amplifier with a low-impedance output driver.

using a differential amplifier with one of the differential inputs grounded. The resistors R_{B1} ($2.46 \text{ k}\Omega$), R_{B2} ($2.46 \text{ k}\Omega$), and R_{E1} (750Ω) set a 2.1 mA of bias current for the common-base stage and the emitter length (l_e) of the input transistor Q_1 is $l_e = 9.04 \mu\text{m}$ (width = $0.2 \mu\text{m}$). With $C_{in} = 0.2 \text{ pF}$, the input return loss is less than -10 dB at $35\text{--}50 \text{ GHz}$ in SPECTRE simulations. The balun amplifier adopts an active inductor load composed of Q_{L1} ($l_e = 1.52 \mu\text{m}$) and R_{L1} (100Ω) to minimize chip area while achieving a tuned gain characteristic with a 3-dB gain bandwidth of $37\text{--}47 \text{ GHz}$ [12]. The equivalent inductance from the active inductor load is 186.5 pH and the parasitic series resistance is roughly 22.8Ω . A 8.2-mA bias current is dedicated to the second stage of a standard differential amplifier, which also has an active inductor load for gain shaping and a resistive degeneration for better linearity. Usually when driving a heavy load, conventional emitter–follower or common-emitter stages suffer from the limited current sourcing or sinking to (or from) the heavy load and this results in a substantial nonlinearity. Therefore, this design adopts a totem-pole technique in the output stage of the balun amplifier so as to drive a low impedance of $\sim 32 \Omega$ (differentially) of the following quadrature all-pass filter, i.e., the emitter–follower $Q_{4,5}$ ($l_e = 3.4 \mu\text{m}$) drives the I/Q network with a finite source impedance and $Q_{3,4}$ ($l_e = 3.4 \mu\text{m}$) assists $Q_{4,5}$ in a push–pull manner, compensating the loss from the finite driving impedance, and hence, maximizing the voltage transfer. $Q_{2,3}$ taps the RF signal through ac coupling ($C_d = 0.5 \text{ pF}$) and R_{E2} (25Ω) is used to linearize $Q_{2,3}$. The current consumption in the output driver is 6 mA and the C_S ($= 50 \text{ fF}$) is an ac-coupling capacitor, also used to resonate any parasitic active inductance caused by the emitter–followers $Q_{4,5}$ at the design frequencies. The balun amplifier shows a peak gain of 12 dB and a minimum NF of $11\text{--}11.5 \text{ dB}$ at $39\text{--}42 \text{ GHz}$. The NF can be improved to $7\text{--}8 \text{ dB}$ with the use of a low-noise common-emitter topology employing inductive degeneration for the matching in the first stage and by replacing the active inductors with passive inductors at the expense of chip area. IIP₃ for the balun amplifier is around -14 dBm at $39\text{--}40 \text{ GHz}$ with a differential $32\text{-}\Omega$ load in SPECTRE simulation.

B. RF Phase Shifter

The integrated RF active phase shifter is shown in Fig. 5 and is based on a phase interpolation between I/Q quadrature signals

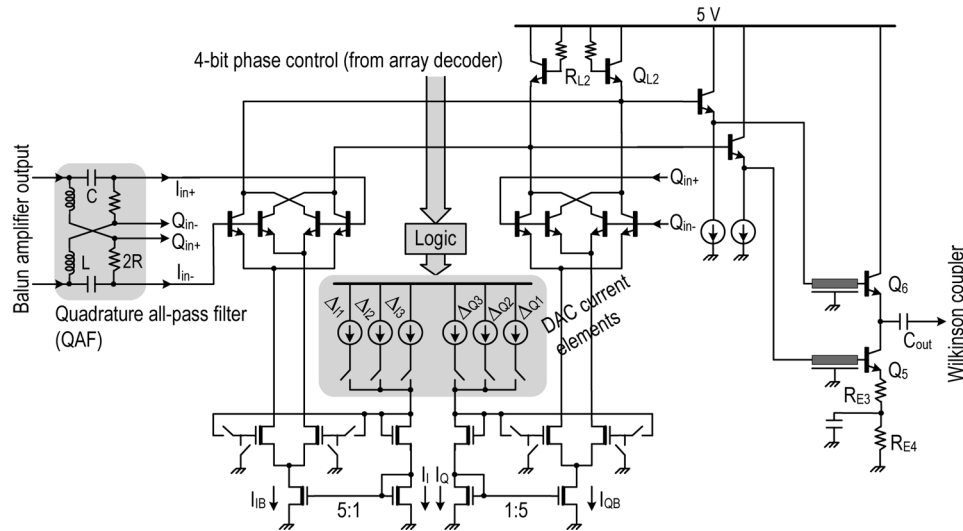


Fig. 5. Circuit diagram of the Q-band 4-bit active RF phase shifter. The input is differential and the output is single-ended.

[6]–[8]. The quadrature all-pass filter generates the differential I/Q signals, which are added together with different weights in the differential vector adder. The adder is a merged configuration of two Gilbert-cell type variable gain amplifiers (VGAs) [8]. The current-steering DAC sets a bias current ratio of $I_I : I_Q$ for the amplitude weightings and the dc control currents are faithfully transferred to the main VGAs (I_{IB} and I_{QB}) by the cascode mirrors with a mirroring ratio of 1 : 5. A control logic encoder generates the necessary digital logic using 4-bit data from the array decoder to control the switches in the DAC and adder.

To increase the I/Q accuracy under a finite loading capacitance (C_L), a low impedance of $\sqrt{L/C} = 27 \Omega$ is chosen for the quadrature all-pass filter: $L = 93.4$ pH, $C = 125.4$ fF, and $2R = 62.5 \Omega$. The I/Q filter exhibits $\leq 5^\circ$ of I/Q phase error at 37–48 GHz under a loading of $C_L = 70$ fF, which includes the base input capacitance from the adder and the parasitic layout capacitance. The output phase error originating from any I/Q amplitude mismatch in the quadrature all-pass filter can be effectively suppressed by optimizing the I/Q amplitude weights accordingly (in other words, by adjusting the DAC currents according to the I/Q amplitude mismatch from the I/Q network). For this, independent current cells are allocated for each I- and Q-path in the DAC and the size of each current element (Δ_{I1-3} and Δ_{Q1-3}) is optimized using SPECTRE simulations to achieve 4-bit phase accuracy with less than ± 1.5 dB of gain variations for all 4-bit phase states.

Theoretically, the bias current ratio of $I_{IB} : I_{QB} = 1 : \sqrt{6}$ results in the minimum phase step of 22.5° bit because of the linear gain dependency on bias current in bipolar transistors ($g_m = I_{bias}/V_T$). However, in reality, the different bias currents modulate the base-emitter diffusion capacitances of the input NPN transistors in the I- and Q-paths differently, and this capacitance variation causes nonnegligible phase error from the required value. Therefore, an optimization is done to set the DAC current elements for the different phase shifts. It is worthwhile to note that, in CMOS, the gate-source capacitance is

fixed as $2/3C_{ox} \times W \times L$ in the first order as long as the transistor operates in saturation mode and the sizing of DAC elements is quite predictable [8], [9]. The emitter length of the input transistors constituting the Gilbert cells is $3.4 \mu\text{m}$. To achieve a wide 3-dB gain bandwidth, the gain characteristic in the phase shifter is staggered from that of the balun amplifier, i.e., the active load composed of Q_{L2} ($l_e = 1.6 \mu\text{m}$) and R_{L2} (100Ω) is optimized for peak gain of 2.5 dB at 34–36 GHz with a 3-dB gain bandwidth of 30–40 GHz. The phase-shifter core including the quadrature all-pass filter and I/Q VGAs provides 7.5 dB of voltage gain, but the output stage loses approximately 5 dB for 50- Ω matching. This results in a 14.5 dB of peak gain at 37–40 GHz with a 3-dB bandwidth of 33–46 GHz for the cascade of active balun and phase shifter.

A class-A totem-pole stage is used for single-ended signal conversion and drives the following Wilkinson coupler (50 Ω). C_{out} (75.4 fF) absorbs a finite parasitic active inductance caused by the emitter-follower Q_6 ($l_e = 3.4 \mu\text{m}$) and improves the impedance matching. The R_{E3} (35 Ω) and R_{E4} (100 Ω) are used for biasing and R_{E3} also increases the linearity of the common-emitter Q_5 ($l_e = 3.4 \mu\text{m}$). The simulated IIP₃ is approximately +6 dBm for the phase shifter core with 0° -bit phase setting and 200- Ω differential loading impedance. The output stage results in an IIP₃ of +9.5 dBm for 50- Ω matching at 39–40 GHz. The current consumption in the phase shifter is 10.5 mA (phase shifter core: 8 mA, totem-pole output stage: 2.5 mA). The overall cascade IIP₃ of the balun amplifier and phase shifter is -16 ± 1.5 dBm at 39 GHz in SPECTRE simulations for all 4-bit phase states. The simulated NF of the phase shifter is 19–19.5 dB, and the cascaded NF of the active balun and phase shifter is 12.7–13 dB at 37.5–44 GHz.

The interconnection transmission lines are in microstrip or grounded coplanar-stripline modes and are characterized as S -parameter sets using full electromagnetic simulations with SONNET [13]. The digital logic is implemented with 0.36- μm CMOS and is compatible with a 3.3-V digital supply voltage.

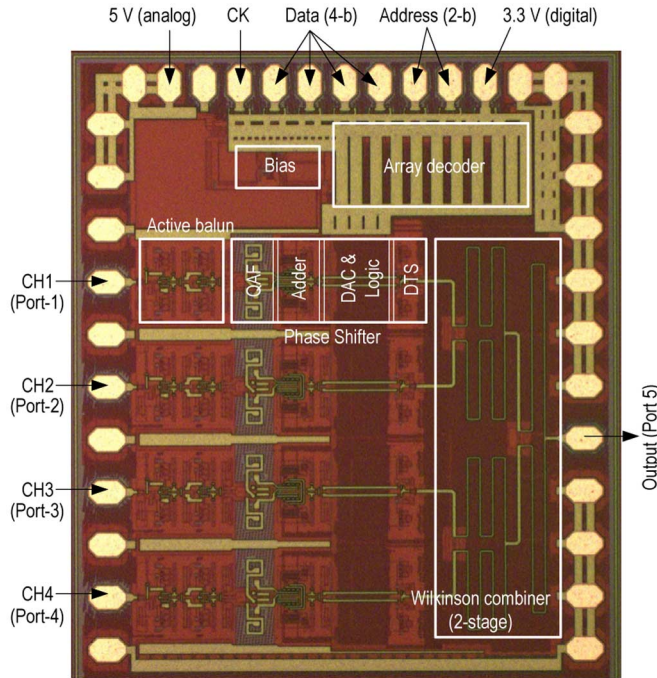


Fig. 6. Q-band phased-array receiver ($1.4 \times 1.7 \text{ mm}^2$).

V. MEASURED RESULTS AND DISCUSSIONS

The phased-array front-end receiver is realized in a $0.18\text{-}\mu\text{m}$ SiGe BiCMOS technology (Jazz SiGe120, SiGe HBT $f_T = 150 \text{ GHz}$). Fig. 6 shows the chip microphotograph and the overall chip size is $1.4 \times 1.7 \text{ mm}^2$. A ground plane (via stack from substrate to top metal) is inserted between each channel and increases the channel-to-channel isolation. The beamformer is measured on chip after a standard short-open-load-thru (SOLT) calibration with a vector network analyzer (Agilent Technologies, PNA-E8364B). The chip consumes 118 mA (29 mA per array element) from a 5-V analog supply voltage.

A. Single-Channel Characterizations

Fig. 7 presents the measured S -parameters of the single path (from CH-1 to Port-5) of the array. The power gain (S_{51}) is shown for all 16 phase states and the average gain per channel is 10.4 dB at 38.5 GHz with a 3-dB gain bandwidth of 32.8–44 GHz. The measured gain is approximately 2.5–3 dB lower than the simulated gain at 30–45 GHz, presumably due to device models and process deviations of the SiGe HBT combined with layout parasitics. The actual measured S_{51} is 4.4 dB and this includes the 6-dB loss in the two-stage Wilkinson combiner since each port of the Wilkinson combiner is terminated with 50Ω . The rms gain error from the average value is $\leq 1.2 \text{ dB}$ at 30–50 GHz for all 4-bit phase states. The input and output return loss (S_{11} and S_{55}) are $\leq -10 \text{ dB}$ at 40–50 GHz and $\leq -8 \text{ dB}$ at 32–50 GHz, and are independent

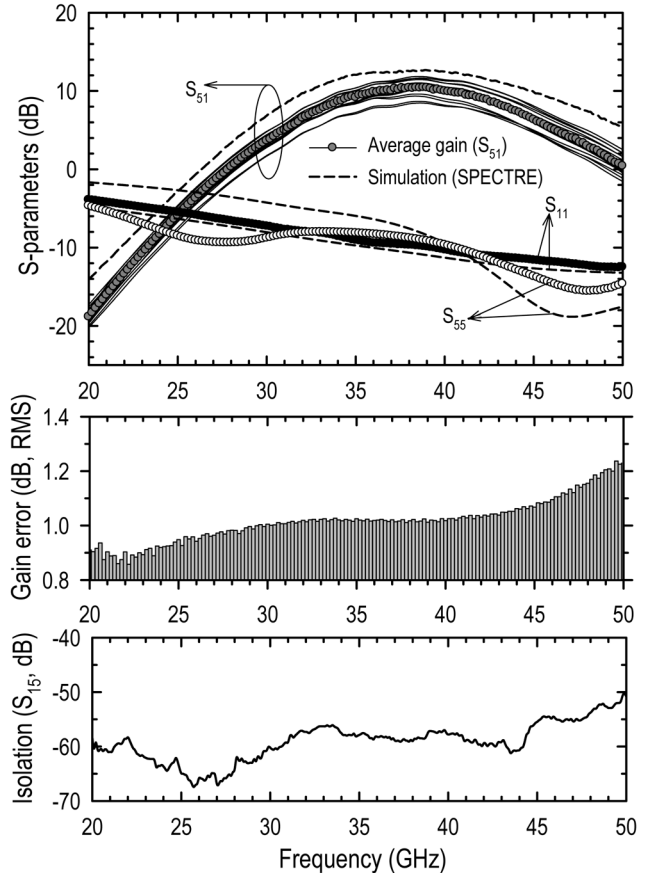


Fig. 7. Measured S -parameters: S_{11} (input return loss), S_{55} (output return loss), S_{51} (power gain) for 16 phase states and S_{15} (isolation), and rms gain error.

of the phase state. The measured output-to-input isolation (S_{15}) is $< -50 \text{ dB}$ up to 50 GHz.

The RF phase shifter shows $\leq 8.7^\circ$ of rms phase error from the ideal phase shift (with reference to the measured 0° bit response) for all 4-bit phase states at 30–50 GHz, achieving 5-bit accuracy (Fig. 8). The phase shift is constant versus frequency when the 0° bit response is subtracted out from the measurements. The calculated group delay from the measured phase response is $85 \pm 3 \text{ ps}$ at 30–45 GHz for all phase states. The constant phase shift is very wideband and is a fundamental aspect of the active phase-shifter approach since the phase interpolation process (adding two orthogonal vectors) is basically independent of the operating frequency. The measured IIP_3 with the 0° bit phase setting is -13.8 dBm and its variation is $\pm 1.5 \text{ dBm}$ at 38.5 GHz for all 4-bit phase states (Fig. 9). The NF, measured with a single-channel test pattern with 0° bit phase setting, is 12.5–14 dB at 37.5–40 GHz (Fig. 10) and is nearly independent on the phase state due to the high gain of the balun amplifier [9]. The higher NF is mainly due to the active inductor loads where internal shot noise sources of NPN HBTs degrade the output noise, as indicated in [9]. To minimize the noise, the active loads should be placed by spiral inductors in practical systems at the cost of the chip area, as mentioned in Section IV.

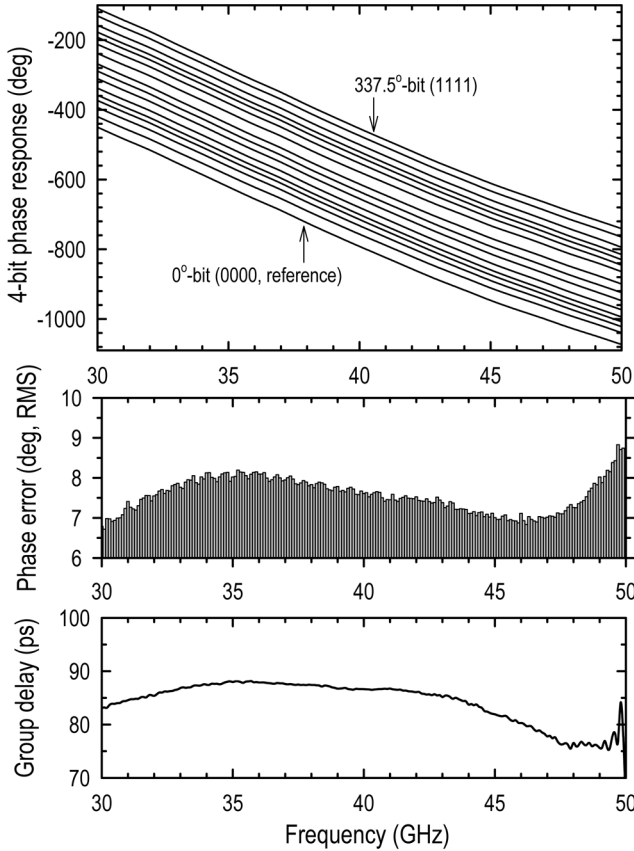


Fig. 8. Measured 4-bit phase response, rms phase error, and group delay for the reference 0°-bit phase state. The group delay is 85 ± 3 ps at 30–45 GHz for all phase states.

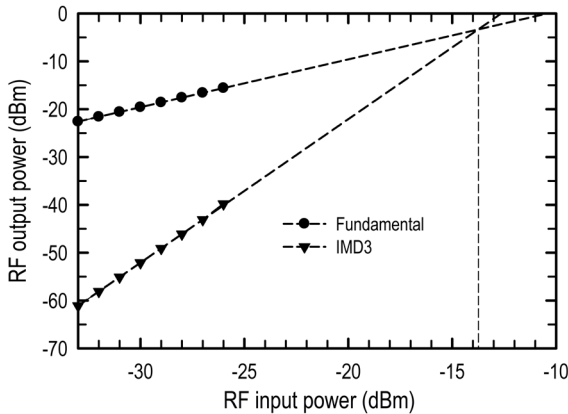


Fig. 9. Two-tone linearity test at 38.5 GHz with 0°-bit phase setting (Channel-1).

B. Array Characterizations

The mismatches (gain and phase mismatches) between the array elements are measured by comparing the 0°-bit (reference) S -parameters of all four channels (S_{51} , S_{52} , S_{53} , and S_{54}). The phased array shows a ≤ 0.4 dB of rms gain variation and a $\leq 2^\circ$ of rms phase mismatch between the channels at 30–50 GHz (Fig. 11). This includes the variation between the different phase shifters and any amplitude and phase imbalance in the two-stage Wilkinson combiner. A -35 -dB measured

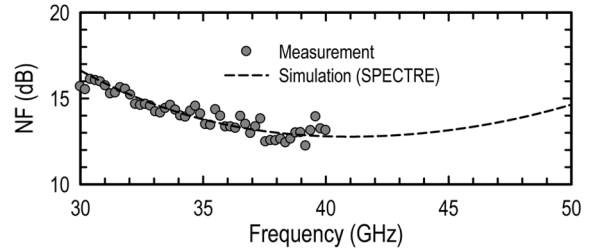


Fig. 10. Measured NF with 0°-bit phase setting (from single-element test pattern including balun amplifier and phase shifter).

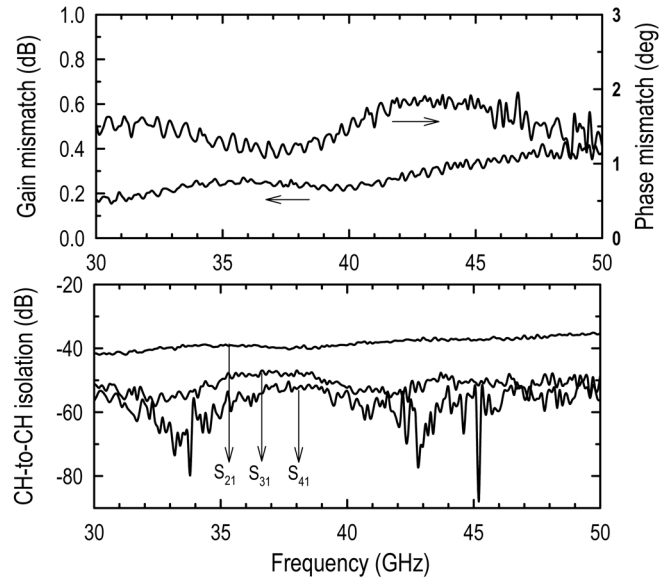


Fig. 11. Measured channel-to-channel mismatch (upper) and isolation (lower).

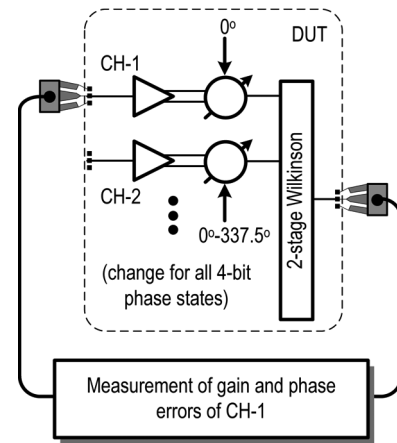


Fig. 12. Coupling test setup.

worst case channel-to-channel isolation occurs between adjacent channels at 30–50 GHz (Fig. 11).

The investigation of the output signal errors (phase and amplitude variations) due to coupling between adjacent channels is important in silicon phased arrays and is detailed in [9] and [14]. Fig. 12 shows the test setup for the measurement of the errors in this study: the phase state of Channel-1 is set as 0°-bit, the phase state of Channel-2 is varied for all 16 phases, and the

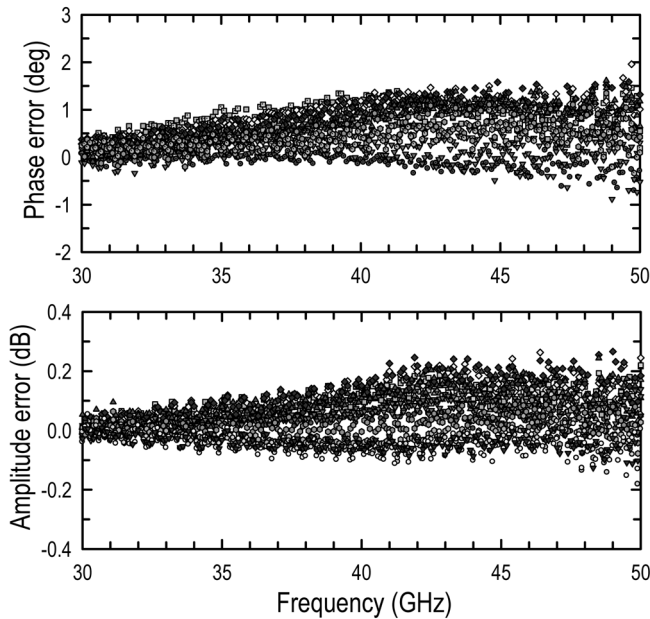


Fig. 13. Measured peak-to-peak phase (*upper*) and amplitude (*lower*) errors from Channel-1 (S_{51}) due to the coupling from Channel-2 in the test setup in Fig. 12.

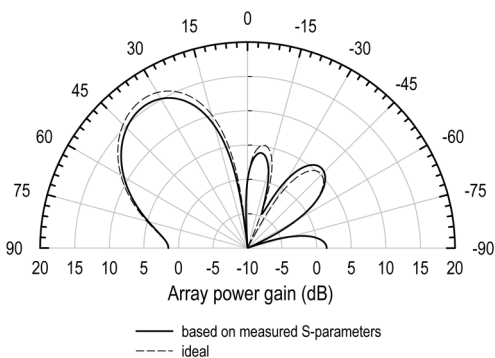


Fig. 14. Simulated array scanning characteristics in ADS based on the measured S -parameters and uniform illumination (35° scan angle).

phase and amplitude variations of S_{51} are measured at the same time. Note that the input port impedance at Channel-2 is set as an open circuit (not loaded with 50Ω) and this results in maximum voltage coupling at Channel-2 and a worst case condition for coupling [14]. The measured peak-to-peak phase error and peak-to-peak amplitude variation in S_{51} are $-1^\circ \sim 2^\circ$ and $-0.2 \sim 0.3$ dB, respectively, at 30–50 GHz for all phase variations of Channel-2. This shows that the phase state of Channel-2 does not affect Channel-1 and is due to the very low on-chip coupling (Fig. 13).

The phased-array pattern (*array factor*) were constructed in ADS at 38.5 GHz using the measured 4-bit S -parameter sets of all four channels under an assumption of a standard linear array ($d = \lambda/2$) with isotropic radiators (Fig. 14). The 35° scan angle from broadside is obtained by applying a progressive phase shift of $103.2^\circ (= 360^\circ/\lambda \times d \sin 35^\circ)$ per element for the ideal case and by applying digitized phase shifts to the nearest 4-bit phase

TABLE I
PERFORMANCE SUMMARY

Quantity	Results
Technology	0.18- μm SiGe BiCMOS (Jazz SiGe120, 1P6M)
Frequency band	Q-Band (3-dB BW: 32.8-44 GHz)
Supply voltage	5 V (analog), 3.3 V (digital)
Current consumption	118 mA (29 mA per channel)
Chip area	$1.4 \times 1.7 \text{ mm}^2$
Single Path Characteristics	
Input return loss	≤ -8 dB @ 32-50 GHz, ≤ -10 dB @ 40-50 GHz
Output return loss	≤ -8 dB @ 32-50 GHz, ≤ -10 dB @ 40-50 GHz
Channel power gain (ave)	10.4 dB @ 38.5 GHz
Phase resolution	4-bit
Gain error	≤ 1.2 dB (rms) @ 30-50 GHz
Phase error	$\leq 8.7^\circ$ (rms) @ 30-50 GHz
Input IP_3	-13.8 dBm @ 38.5 GHz
NF	*12.4 dB @ 38.5 GHz
Group delay	85 ± 3 ps @ 30-45 GHz
Isolation (output-to-input)	≤ -50 dB @ 30-50 GHz
Array Characteristics	
Phase mismatch (rms)	$\leq 2^\circ$ @ 30-50 GHz (between all channels)
Amplitude mismatch (rms)	≤ 0.4 dB @ 30-50 GHz (between all channels)
Isolation (channel-to-channel)	≤ -35 dB @ 30-50 GHz (between all channels)
Array factor directivity	6 dB (4 elements)

* The NF can be improved to 7-8 dB with the use of a different low-noise active balun design (see text).

states. The result is close to the ideal case due to the low rms gain error and phase mismatch between the four channels.

The measured results are summarized in Table I.

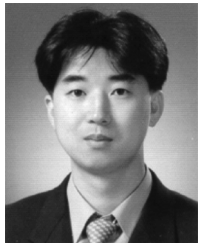
VI. CONCLUSIONS

This paper has demonstrated a four-element phased-array receiver in a 0.18- μm SiGe BiCMOS technology for Q-band (30–50 GHz) satellite communications and radar systems. The design is based on the *all-RF* architecture with 4-bit RF active phase shifters in a corporate-feed approach, and using a compact two-stage Wilkinson power-combiner network. The chip also contains all the CMOS digital circuits necessary for complete control of the phased array. The integrated phase shifter shows very linear constant phase shift over 30–50 GHz (group-delay variation ≤ 10 ps @ 30–50 GHz) with 5-bit phase accuracy. The typical loss of the on-chip Wilkinson coupler is 0.6 dB up to 50 GHz. Measurement done on all four channels shows very low rms phase and gain errors over the 4-bit phase states both in a single channel and also between the four different channels. The *all-RF* architecture provides good scalability to large arrays with a simple system architecture, and the design can be extended to 60 or 77 GHz for low-cost phased arrays.

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