

Statistical Modeling With the PSP MOSFET Model

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Abstract—PSP and the backward propagation of variance (BPV) method are used to characterize the statistical variations of metal-oxide-semiconductor field effect transistors (MOSFETs). BPV statistical modeling of NMOS and PMOS devices is, for the first time, coupled by including self-consistent modeling of ring oscillator gate delays. Parasitic capacitances are included in the analysis. The proposed technique is validated using Monte-Carlo simulations and by comparison to experimental data from two technologies.

Index Terms—Backward propagation of variance, PSP model, statistical modeling.

I. INTRODUCTION

STATISTICAL modeling is critical to the design of modern integrated circuits (ICs) to ensure high product yield [1]–[4]. The surface-potential based PSP metal-oxide-semiconductor field effect transistors (MOSFET) model [5], [6] provides a unique and simple capability to physically link fluctuations in device electrical performances to variations in a small number of fundamental process parameters. This is in contrast to MOSFET models that are based on a large number of empirical parameters, for which data driven numerical procedures are often required for statistical modeling.

This paper presents a unified and extendable method to extract the statistics of PSP parameters directly from electrical test (ET) data. The procedure leverages the physical nature of the PSP model and uses backward propagation of variance (BPV) method [7]–[9]. The BPV procedure is expanded to characterize circuit performances as well as individual NMOS and PMOS transistor performance.

We compare results of our procedure against ET data that includes DC, capacitance, and ring oscillator (RO) gate delay measurements from two 0.18 μm CMOS technologies from

Manuscript received February 27, 2008; revised November 25, 2008 and July 9, 2009. Current version published March 19, 2010. This work was supported in part by the Semiconductor Research Corporation, under Contract no. 2006-VJ-1450. This paper was recommended by Associate Editor, M. Orshansky.

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Digital Object Identifier 10.1109/TCAD.2010.2042892

two different manufacturers. These results are verified using Monte-Carlo simulations.

Compared to previous applications [7]–[9] of the BPV method, this paper introduces two new developments. First, characterization of NMOS and PMOS devices is coupled. Traditionally NMOS and PMOS transistors are statistically characterized separately. This does not guarantee accurate statistical modeling of circuit performances that depend on both NMOS and PMOS devices. In this paper, RO delay is included as a circuit level performance to be modeled, which couples to, and is strongly correlated with, the characteristics of both NMOS and PMOS devices [10]–[12]. Thus, in contrast to earlier work, our approach combines electrical measurements both of individual device characteristics and of circuit performance to develop a unified and practical way to characterize the variations in circuit delays. We also found that it can be difficult to model statistical variations accurately over all biases by BPV fitting of electrical performances at only one DC bias. The situation can be improved by including electrical performances over bias as statistical modeling targets. This can be easily achieved with our proposed procedure. For instance, in our experiment the variation of RO delay versus supply voltage was successfully fitted by targeting not just the variance of the saturated drain current at maximum gate bias but by (least squares) fitting the additional drain current variances at several gate biases (with minimal loss in accuracy of modeling at the highest gate bias).

The second new feature of the present investigation is that the process parameters are selected directly from the parameter list of the PSP model. Due to limited physical content in some older compact MOSFET models, mappings have to be set up to link the process parameters and the actual compact model parameters. In PSP several of the model parameters (e.g., TOXO, VFBO, NSUBO) have direct relations to process variations and no external mappings need to be introduced for statistical modeling.

We note that the method described in this paper is applied to characterize the global (geometry-independent) component of variation; the reason we present results from 0.18 μm technologies is because for these technologies global variation dominates the mismatch (or local, geometry-dependent) component of variation. For more advanced technologies, where mismatch becomes more important, one can extract the mismatch and global variations in subsequent steps [8]. First, mismatch variation is characterized based on mismatch measurements [9]. Then the global variation is obtained by

subtracting the mismatch variation from the total observed fluctuations in each electrical performance

$$\sigma_{ei,global}^2 = \sigma_{ei,total}^2 - \sigma_{ei,local}^2 \quad (1)$$

The extraction of global variation then proceeds as described in the following sections.

II. METHOD

Much work has been devoted to investigate the nature of process variations and their effects on the performances of the individual MOS transistors [13]–[15]. For MOSFETs, the process variations that impact circuit functionality the most are oxide thickness (T_{ox}), effective channel length (L_{eff}) and width (W_{eff}), flatband voltage (V_{fb}), and substrate doping (N_{sub}). Variations in these process parameters affect electrical performances such as threshold voltage (V_{th}), saturated drain current (I_{dsat}), gain factor ($\beta = \mu_0 C_{ox} W/L$) and gate delay (t_d). Although it is important to understand the physics and mechanisms that cause variations in device characteristics, the ultimate goal of statistical modeling is to accurately represent variations of circuit performances. Hence, extracting the variations of the process parameters from wafer-level data via a physical compact model (i.e., using the BPV method) is a natural approach for statistical modeling [7], [8].

Let e_i ($i = 1, 2, \dots, m$) be measures of electrical performance (i.e., V_{th} , I_{dsat} , etc.) for a MOSFET and p_j ($j = 1, 2, \dots, n$) be process parameters (e.g., T_{ox} , L_{eff} , etc.). Taylor expansion of e_i in the neighborhood of $\bar{\mathbf{p}} = (\bar{p}_1, \bar{p}_2, \dots, \bar{p}_n)$ gives

$$e_i \approx e_i(\bar{\mathbf{p}}) + \sum_{j=1}^n s_{i,j} (p_j - \bar{p}_j) \quad (2)$$

and sensitivity analysis yields

$$\sigma_{e_i}^2 = \sum_j s_{i,j}^2 \sigma_{p_j}^2 \quad (3)$$

where

$$s_{i,j} = \left. \frac{\partial e_i(\mathbf{p})}{\partial p_j} \right|_{\mathbf{p}=\bar{\mathbf{p}}} \quad (4)$$

and $\sigma_{e_i}^2$ and $\sigma_{p_j}^2$ are the variances for e_i and p_j , respectively. There are two assumptions that underlie (2): that the process parameters are independent; and that the variations in the parameters should be small so that the electrical performances are well approximated as linear functions of process parameters. Parameter correlations can be handled by decomposing them into physical combinations of common and independent components, to provide a completely independent set of modeling parameters [16]. An extension to handle nonlinearities in the $e_i(\mathbf{p})$ mappings is reviewed in Section V, but as our results below show, this is not important for the devices we analyze.

For m electrical performances and n process parameters (treated as model parameters), this results in an $m \times n$ linear system

$$\sigma_e^2 = \mathbf{S} \sigma_p^2 \quad (5)$$

where

$$\sigma_e^2 = [\sigma_{e_1}^2, \sigma_{e_2}^2, \dots, \sigma_{e_m}^2]^T \quad (6)$$

$$\sigma_p^2 = [\sigma_{p_1}^2, \sigma_{p_2}^2, \dots, \sigma_{p_n}^2]^T \quad (7)$$

and the sensitivity matrix is

$$\mathbf{S} = \left[\left(\frac{\partial e_i}{\partial p_j} \right)^2 \right]_{i=1,2,\dots,m; j=1,2,\dots,n} \quad (8)$$

For $m = n$ the variances of each process parameter can be found by directly solving (5). A least squares fit is used when $m > n$. Note that for some process parameters and figures of merit the variations are normalized to percentage values; for clarity and convenience of notation variations are expressed here in absolute terms.

III. EXPERIMENT

The method described in the previous section was applied to two 0.18 μm CMOS technologies. The ET data was taken from scribe grid process control (SGPC) monitors located between dice throughout the wafers. Various test structures were available, including several geometries of MOSFETs, diodes, and capacitors, some mismatch structures, and some ring oscillators. These enable monitoring and characterization of the statistical variations of the process. The number of devices measured from the sample wafers was: 448 MOSFETs, 112 oxide capacitance structures, 112 diodes, and 56 ring oscillators. These sample sizes are sufficient to characterize the statistical variations and correlations of the electrical performances.

The DC currents of the MOSFETs and the capacitances of the junctions were measured on a standard probe station. Figures of merit that affect digital circuit performance were selected as key quantities and were extracted from the raw data. For example, the saturated drain current of a short channel device is highly correlated with the switching speed of digital circuits. Hence, it is chosen as one of the e_i in (2). The selections of all e_i for both types of devices are listed in Table I. The PSP model parameters used for statistical modeling are listed in Table II. Note that in our experiment, the body effect was not characterized and its dependence on N_{SUB} is weaker than on T_{ox} , so we did not include NSUB as a process parameter. Rather, V_{th} at zero body bias was modeled through the flatband voltage VFBO. Note also that length dependent threshold voltage (VFBL) is an independent parameter to model the variation of VFB for short channel devices, in addition to the effect of channel length variations

TABLE III
STANDARD DEVIATIONS EXTRACTED USING THE BPV METHOD

p_j	NMOS		PMOS		Unit
	Nominal	1σ	Nominal	1σ	
TOXO	4.158	0.02	4.083	0.02	nm
VFBO	-1.031	0.00323	-1.138	0.0022	V
VFBL	-0.04347	0.0	-0.056	0.00053	-
UO	0.0608	0.00111	0.01855	0.00061	$m^2/V/s$
LAP	22.12	3.682	20.37	2.93	nm
WOT	0.0	3.103	-16.72	3.179	nm
VFBW	0.0	0.00391	-0.013	0.00187	-
VFBLW	-0.002	0.00089	0.00458	0.001	-

can go over a ‘cliff’ as a parameter gets pushed to an extreme value; a sensitivity calculated from a small perturbation would not catch any problems that could arise if a parameter was at an extreme. We emphasize that each element of the sensitivity matrix is evaluated using full SPICE simulation including for the RO delay, i.e., the PSP model and complete RO netlist are simulated to guarantee that the accuracy of the sensitivities is not compromised. This also allows the physical content of the PSP model to be fully leveraged, as described in Section I as one of the main reasons to initialize this paper.

The extracted parameter statistics are listed in Table III. Note that during the extraction procedure it was found that the parameter LAP was sufficient to fit the variations for short channel NMOS devices. VFBL was not needed and therefore its standard deviation is listed as zero in Table III. The fact that PSP needs one less parameter than usual for statistical modeling underscores the physical nature and accuracy of PSP, and highlights the benefit of PSP for statistical modeling.

An advantage of the proposed method is that it is extendable and the solution it generates is self-consistent. For example, additional circuit topologies and process parameters, defined to target specific circuit types, can be added and (9) is easily expanded. It is worth pointing out that the approach proposed has no presumption on which effect is dominant in the process. In fact, the BPV procedure is generic and suitable for all processes irrespective of their state of maturity. In this paper, L_{eff} variation is the largest contributor to gate delay variation, because the ring oscillators use minimum channel length devices. Projections of the variations are not needed for BPV; variations in any number of parameters are handled by the procedure.

IV. VERIFICATION

The validity of the proposed method was verified by generating 5000 Monte-Carlo samples based on the extracted statistical models. The Monte-Carlo simulations were done by randomly generating samples of each process parameter based on independent Gaussian distributions defined by the parameters listed in Table III. The full PSP model was used for simulation and the statistics of the electrical performances were calculated based on circuit simulations for each sample of process parameter values. Fig. 1(a) and (b) shows the results for V_{tr} variations for large NMOS devices and I_{ds} for

TABLE IV
STANDARD DEVIATIONS OF THE MONTE-CARLO SIMULATION RESULTS
COMPARED WITH THOSE OF MEASUREMENTS

	e_i	NMOS		PMOS		Unit
		Meas. σ	Sim. σ	Meas. σ	Sim. σ	
Large	V_{tr}	3.9	4.0	3.5	3.5	mV
Short	V_{ts}	14.5	14.2	12.7	12.6	mV
	I_{ds}	2.13	2.32	3.37	3.42	%
Narrow	V_{tn}	16.8	17.0	8.3	8.3	mV
Small	V_{tm}	26.0	26.0	21.6	21.6	mV
	I_{dm}	4.28	4.25	5.98	5.99	%

short NMOS devices, respectively. The complete results are listed in Table IV; the simulated variations closely match the original measurements, verifying the validity and accuracy of our approach. More importantly, because the PSP simulations inherently include the full effect of nonlinearities the closeness of the measured and simulated results verifies our assertion that the linear analysis of Section II is applicable.

Similarly good results were obtained when our method was applied to another $0.18\mu\text{m}$ technology (Jazz SBC18 SiGe BiCMOS, denoted as technology B) from a different manufacturer, using the same selection of process parameters and electrical performances. Fig. 2 shows simulation results for electrical performances for short channel NMOS devices (note that only the $\pm 3\sigma$ limits were available from the measurements).

For the RO delay, two contributing factors are considered. One is the DC performances of the MOSFETs, which have been already verified (see Table IV). Another comes from the parasitics, i.e., the junction and interconnect capacitances. Because the layout of the RO structure under test is compact, the variation of the interconnect capacitance was neglected. But the nominal values of the interconnect capacitances were extracted using the Cadence Assura-RCX tool to make the simulations as accurate as possible. The influence of the junctions was taken into account by measuring the variation of the zero-bias capacitances for large square diodes, which are used to characterize the bottom (area) component of the junction capacitance. The gate-edge and STI-edge components are small and so variations in them were neglected for simplicity. Using the JUNCAP2 model [17], the zero-bias capacitance C_{JO} can be approximated as

$$C_{\text{JO}} = A \cdot \text{CJORBOT} \quad (10)$$

where CJORBOT is the JUNCAP2 parameter for zero-bias capacitance per unit area and A is the area of the diode. Hence

$$\sigma_{\text{CJORBOT}} = \frac{\sigma_{C_{\text{JO}}}}{A}. \quad (11)$$

The extracted statistics are listed in Table V.

Monte-Carlo simulations were performed with and without the extracted junction statistics. The results are shown in Fig. 3 and listed in Table VI. The simulated standard deviations match the ET data well. Notice that the contribution of the junction capacitance variation is small in this case. If

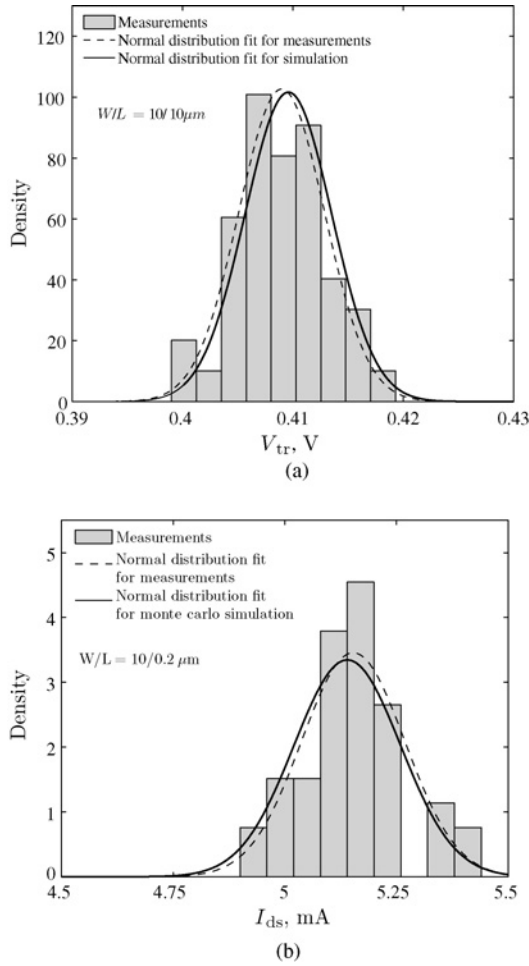


Fig. 1. Monte-Carlo simulation results comparison to measurements. (a) Threshold voltage for large NMOS devices. (b) Saturated drain current for short NMOS devices.

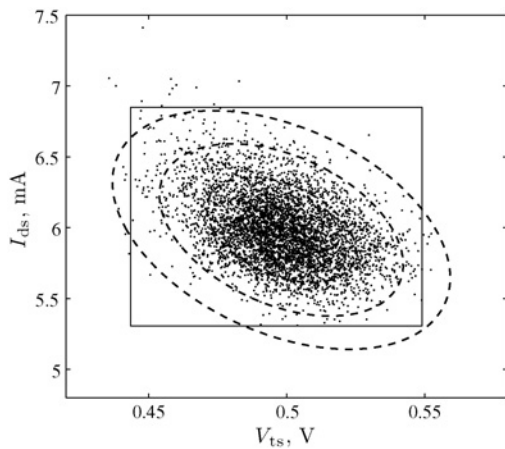


Fig. 2. Simulation results for small devices ($W/L = 10/0.18 \mu\text{m}$) for technology B compared to measurements. Symbols are Monte-Carlo simulations and dashed lines represent the contour ellipses for a bivariate normal distribution corresponding to probabilities of 0.683, 0.954, and 0.9973 (i.e., to deviations of less than 1σ , 2σ , and 3σ when interpreted in terms of single normal random variable). The solid box represents $\pm 3\sigma$ limits for each variable from measurements.

TABLE V

STANDARD DEVIATIONS EXTRACTED FOR JUNCTION CAPACITANCES

p_j	NMOS		PMOS		(Unit)
	Nominal	1σ	Nominal	1σ	
CJORBOT	1.344	0.033	1.37	0.010	mF/m^2

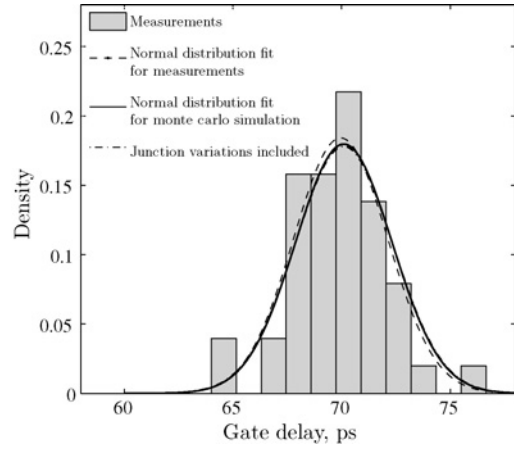


Fig. 3. Monte-Carlo simulation results for RO delay compared with the measurements.

TABLE VI

STANDARD DEVIATIONS OF THE MONTE-CARLO SIMULATION RESULTS FOR RO DELAY COMPARED WITH THOSE OF MEASUREMENTS

	Spec.	Meas.	W/O Junctions	W/ Junctions	Unit
RO	t_d	2.17	2.15	2.21	ps

otherwise, it can be included in the formulation based on (9) similarly to other electrical performances.

An important feature of our method is that the relative contribution of the variation in each process parameter to the overall variation of each electrical performance can be easily determined. For instance, the overall gate delay variance is

$$\left(\frac{\sigma_{t_d}}{t_d}\right)^2 = \left[\frac{1}{t_d} \cdot \frac{\partial t_d}{\partial \text{VFBO(N)}}\right]^2 \cdot \sigma_{\text{VFBO(N)}}^2 + \dots + \left[\frac{1}{t_d} \cdot \frac{\partial t_d}{\partial \text{VFBO(P)}}\right]^2 \cdot \sigma_{\text{VFBO(P)}}^2 + \dots \quad (12)$$

Each term on the right-hand side of this expression was calculated and the major factors are listed in Table VII. Not surprisingly, about 90% of the gate delay variation comes from variations in mobility and effective channel length, because these most affect the device performances that determine the gate delay of ring oscillators. Note also that the variation of PMOS device process parameters has more impact on gate delay than variations of NMOS device process parameters, which indicates that the low-to-high transition dominates the high-to-low transition for gate delay for these specific ring oscillators.

To further demonstrate the capability of this method we carried out another experiment to model the variation of the gate delay as a function of supply voltage. Fig. 4 shows the trajectories of the drain current of the NMOS device in an inverter for various supply voltages. When lowering the

TABLE VII
DEVICE CONTRIBUTION FOR THE GATE DELAY

	NMOS		PMOS	
	UO	LAP	UO	LAP
Contributions	7%	16%	20%	51%

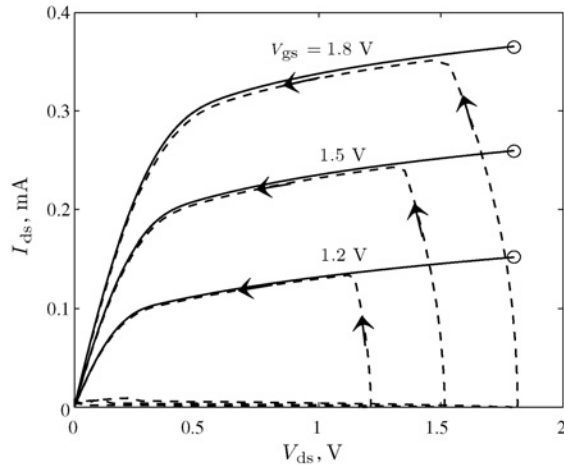


Fig. 4. Simulated trajectories of the drain currents for a NMOS in an inverter mapped on the traditional IV characteristics. The solid and dashed lines are the IV curves and the trajectories, respectively, for a short channel NMOS for different gate biases. The locations where their variations are used in extraction are marked by the round symbols.

supply voltage, the output voltage lowers correspondingly. Generally, two factors affect the overall variation of the RO delay: the load capacitance and the drive current. The results presented above show that the gate and junction capacitance variations have only a small contribution to the overall gate delay variation. The saturation current is thus the dominant factor controlling gate delay variation and σ_{t_d} increases as the supply voltage goes down. To accurately model the variation of RO delay as the supply voltage changes it is therefore necessary to accurately model the variations of the NMOS and PMOS saturation currents for various supply voltages, which requires adding these to (9). For simplicity we use a drain-source voltage (V_{ds}) of 1.8V and several gate bias (V_{gs}) values, because the drain current does not vary much with V_{ds} in saturation.

Here we add I_{ds} at $V_{gs}=1.0$ and 1.4-V for both types of devices. With the inclusion of these electrical performances in (9) the extraction was repeated and a new set of variances for the process parameters was obtained. 5000 Monte-Carlo simulations were performed again for verification. Fig. 5 shows the simulated standard deviations of the saturation currents as a function of gate bias for both extractions (with only a single drain current being fitted, and with drain current for three gate biases being fitted). The measured variation of the gate delay versus supply voltage is also shown in Fig. 6. As can be seen, the simulated results using statistics extracted at only high gate bias (see Table III) match the measurements at this bias ($V_{gs} = 1.8$ -V), but underestimate the variations for lower gate biases. By adding the variances of additional electrical performances (currents at lower gate

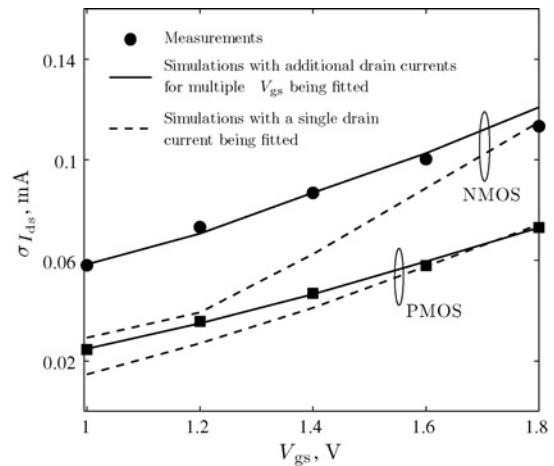


Fig. 5. Simulated standard deviations for the saturation currents for various gate biases compared with the measurements.

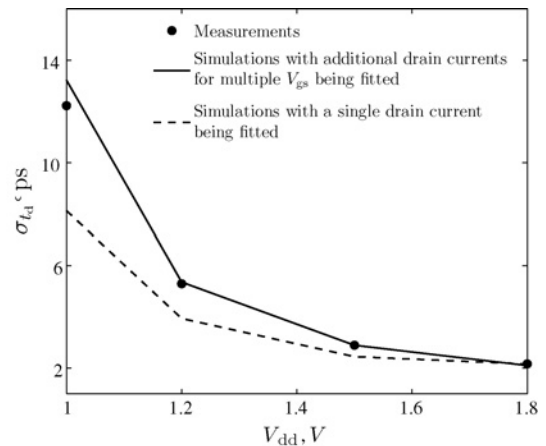


Fig. 6. Simulated standard deviations for RO gate delay for various supply voltages compared with the measurements.

voltages) as targets to model, the simulated results for the bias dependent variation of gate delay and of drain current for both NMOS and PMOS devices are automatically captured. This reinforces the accuracy, effectiveness, and extensible nature of our method; the gate delay variations for supply voltages other than 1.8V were *not* included as fitting targets. Note that because the number of electrical performances is greater than the number of the process parameters, a least squares fit was used in solving (9) and nonzero residuals between simulated and measured σ_{e_i} are therefore expected, in contrast to the case $m = n$ when the residuals should be zero. Table VIII compares simulated results with the measurements (cf. Table IV). In this experiment, the extracted statistics produced better results for bias dependent variations but less accurate results for V_{ts} . This is expected since LAP and VFBL were reconciled to fit bias dependent quantities for short channel devices. If “exact” matches are desired, a square sensitivity matrix is preferred. But this can restrict the overall scope of statistical modeling accuracy.

TABLE VIII
STANDARD DEVIATIONS OF THE MONTE-CARLO SIMULATION RESULTS
USING ADDITIONAL ELECTRICAL PERFORMANCES (CF. TABLE IV)

	e_i	NMOS		PMOS		Unit
		Meas.	Sim.	Meas.	Sim.	
Large	V_{tr}	3.9	4.0	3.5	3.4	mV
Short	V_{ts}	14.5	16.4	12.7	17.8	mV
	I_{ds}	2.13	2.33	3.37	3.33	%
Narrow	V_{tn}	16.8	17.0	8.3	8.2	mV
Small	V_{tm}	26.0	26.1	21.6	22.2	mV
	I_{dm}	4.28	4.26	5.98	6.10	%

V. DISCUSSION ON MODELING NONLINEARITY

One underlying assumption in our method is that the variations in the electrical performances can be approximated as linear functions of process parameters [see (3)]. A quadratic version of the BPV method [18] can be used when the variations of the process parameters are large and it becomes necessary to model the nonlinearity. Instead of (2), a second degree term can be kept when expanding e_i , that is

$$e_i \approx e_i(\bar{\mathbf{p}}) + \sum_{j=1}^n s_{i,j}(p_j - \bar{p}_j) \quad (13)$$

$$+ \sum_{j,k=1}^n s_{i,jk}(p_j - \bar{p}_j)(p_k - \bar{p}_k) \quad (14)$$

where $s_{i,j}$ is defined in (4) and

$$s_{i,jk} = \frac{\partial^2 e_i(\mathbf{p})}{\partial p_j \partial p_k} \Big|_{\mathbf{p}=\bar{\mathbf{p}}} \cdot \quad (15)$$

After some algebra, one has

$$\mu_{e_i} \approx e_i(\bar{\mathbf{p}}) + \sum_{j=1}^n s_{i,jj} \sigma_{p_j}^2 \quad (16)$$

and

$$\sigma_{e_i}^2 \approx \sum_{j=1}^n s_{i,j}^2 \sigma_{p_j}^2 + 2 \sum_{j,k=1}^n s_{i,jk}^2 \sigma_{p_j}^2 \sigma_{p_k}^2. \quad (17)$$

Therefore, instead of a linear system, one has to solve numerically a set of nonlinear equations [18]. However, in our experiment the nonlinearity is not significant and we find that the linear model is sufficient to model all of the observed electrical performances, as shown by the validation results in Section IV.

VI. CONCLUSION

The PSP model and the BPV method have been combined for statistical modeling of two different technologies. The effect of parasitic capacitance was taken into consideration in our analysis, although its impact on RO gate delay was shown to be small for the circuits and technologies that were investigated. Our results were verified by comparing Monte-Carlo simulations to ET data. The new approach to statistical

modeling presented here shows that accurate statistical modeling with a small number of statistical parameters is enabled by the strong physical basis of the PSP model. We also show that overall statistical modeling accuracy can be improved, at the expense of some loss in accuracy of ‘point’ modeling, by using an over-determined formulation, i.e., by including more electrical performances to fit than process parameters used for modeling.

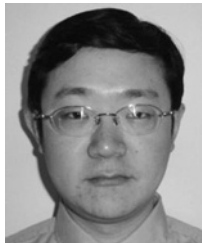
ACKNOWLEDGMENT

The authors are grateful to Y.-B. Park, I.-S. Lim, A. Zlotnicka, D. Bush, C. MacKenzie, and W. Brown, of Freescale Semiconductor, for their expertise, help with lab measurements and characterization, and to I. To and D. Morgan, of Freescale Semiconductor, for their providing the sample wafers and technical documentations.

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