

A Ku -Band Two-Antenna Four-Simultaneous Beams SiGe BiCMOS Phased Array Receiver

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Abstract—This paper presents a Ku -band SiGe BiCMOS phased array receive chip capable of forming four-simultaneous beams from two antenna inputs. The design is based on the all-RF architecture with 4-bit active phase shifters and 4-bit variable gain amplifiers in each channel. The four-beam chip results in a gain of 4–6 dB per channel at 13–15 GHz, a noise figure of 10–11 dB, a worst case input $P_{1\text{ dB}}$ of -14.3 dBm per channel (input third-order intercept point of -7 dBm), and an rms phase and gain error of $< 12^\circ$ and 1.5 dB, respectively. A gain control of 17 dB is also achieved with a phase change of $< 5^\circ$. The four-beam chip was tested using two input signals and results in a gain of 9–11 dB at 13–15 GHz. The on-chip isolation between the channels has been fully characterized and is > 40 dB at 13–15 GHz. The chips can operate over an instantaneous bandwidth of > 1 GHz at any frequency from 13 to 15 GHz, and the four beams can be at the same frequency if required. With all digital control circuitry and electrostatic discharge protection for all I/O pads, the chip occupies an area of 2.4×4.3 mm² and consumes 520 mA at 3.5-V supply voltage. To our knowledge, this is the first demonstration of an all-RF phased array silicon chip capable of producing four-simultaneous beams from two different antennas or four-simultaneous beams of different polarizations from a dual polarization antenna. The application areas are in satellite communications and defense systems.

Index Terms—Multibeam, phased array, phase shifter, SiGe BiCMOS.

I. INTRODUCTION

PHASED arrays based on silicon RF integrated circuits (RFICs) are being developed as a lower cost solution due to their high integration density, yield, and functionality on a single chip. Recently, phased arrays based on all-RF phase shifting [1]–[10], IF or baseband phase shifting [11], [12], and local oscillator (LO) phase shifting [13], [14] have been realized in standard CMOS and SiGe technologies. The all-RF architecture has been demonstrated from X - to W -band using

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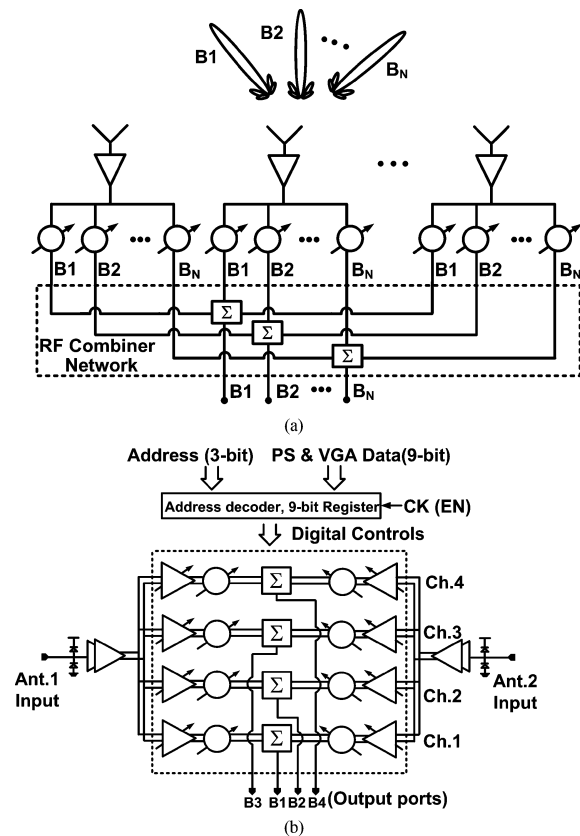


Fig. 1. (a) Multibeam phased array receiver based on all-RF architecture, and (b) proposed single-chip two-antenna phased array receiver with 4 simultaneous beams.

single element or four, eight, or 16 elements on a single chip in transmit or receive configurations [2]–[5]. A four-element transmit/receive chip with 5-bit amplitude and phase control was also recently demonstrated at 36–38 GHz [1]. This not only reduces the number of chips to be assembled in the phased array, but also simplifies the digital control-line distribution in large arrays.

A natural progression of this work is the integration of multiple simultaneous beams on a single chip. This has been demonstrated using GaAs chip-sets [15], and recently using the LO phase-shifting approach, but with some limitations—the beams could not all operate at the same frequency and had limited instantaneous bandwidths [16]. A phased array receiver capable of two-simultaneous beams was demonstrated using an SiGe process [17]. The multibeam design presents special challenges since high isolation is required between the beams. The beams should also be able to operate at different frequencies, or at the same frequency, and with a wide instantaneous bandwidth.

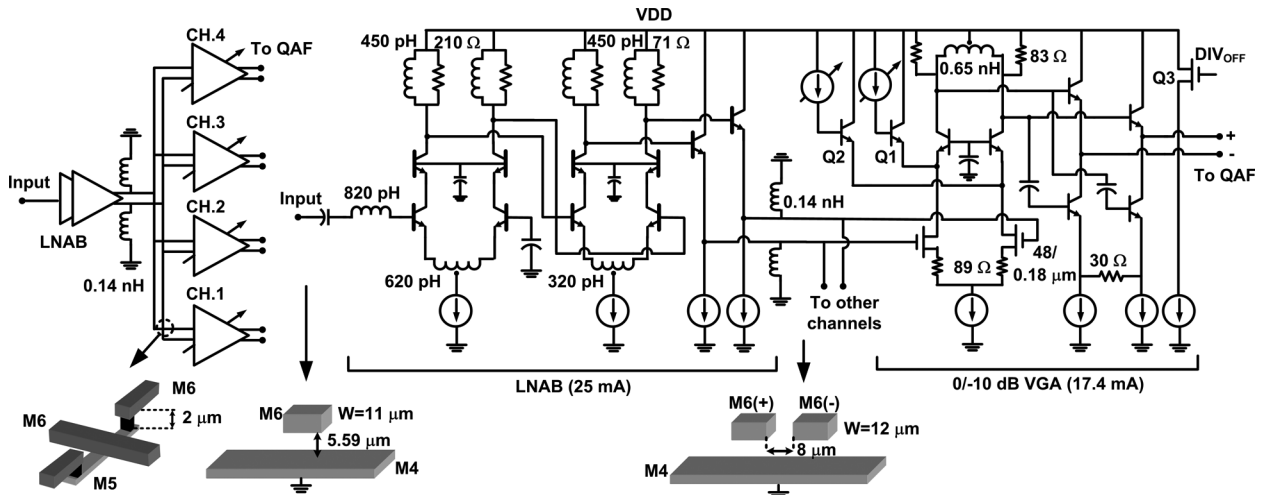


Fig. 2. Block and circuit diagrams of LNAB, 1:4 distribution network, and the 0/ - 10-dB VGA.

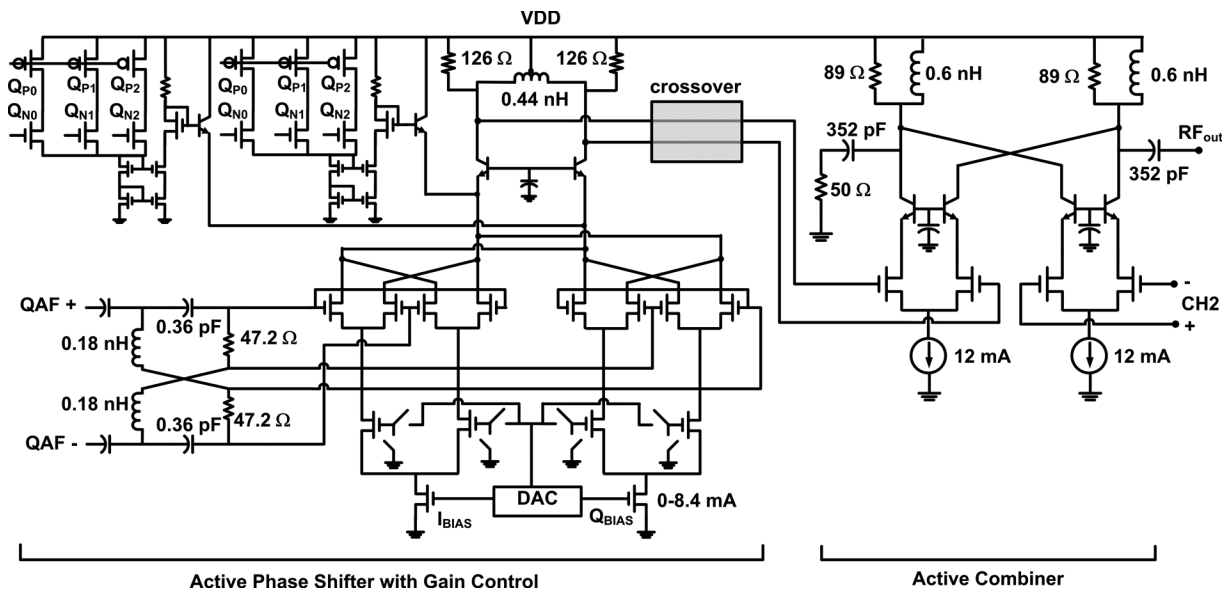


Fig. 3. Circuit diagram of active phase shifter and active combiner.

In this paper, a two-antenna input phased array receiver capable of generating four-simultaneous beams is demonstrated in a SiGe BiCMOS process using the all-RF phase-shifting architecture. The chip can also be connected to a single antenna with two different polarization ports, therefore allowing the formation of four simultaneous beams each of a different polarization. The application areas are in low-cost phased array for *Ku/Ka*-band mobile satellite [18] and radar systems.

Fig. 1(a) presents a generic rendering of a phased array with simultaneous beam capabilities and the corresponding layout of the silicon chip with two-antenna inputs. The input signal from each antenna is divided into four different paths (or channels) each with its own phase and amplitude control. The corresponding signals from each path are then added to synthesize the multiple simultaneous output beams. This is typically done in a multilayer beam-forming network, which occupies a lot of space in a phased array system. The interaction between the different paths (channels) should be ideally zero, and the phase and

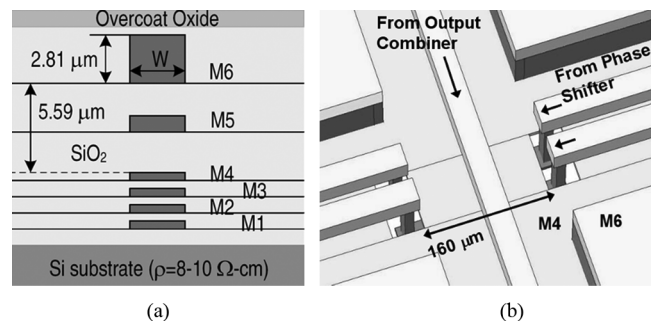


Fig. 4. (a) Metal-stack layers of the Jazz Semiconductor SBC18HX process. (b) Crossover structure after the active combiner.

amplitude setting in one beam cannot affect the performance of the other beams. The silicon design integrates all these functions into a single chip while still maintaining excellent isolation between the output beams.

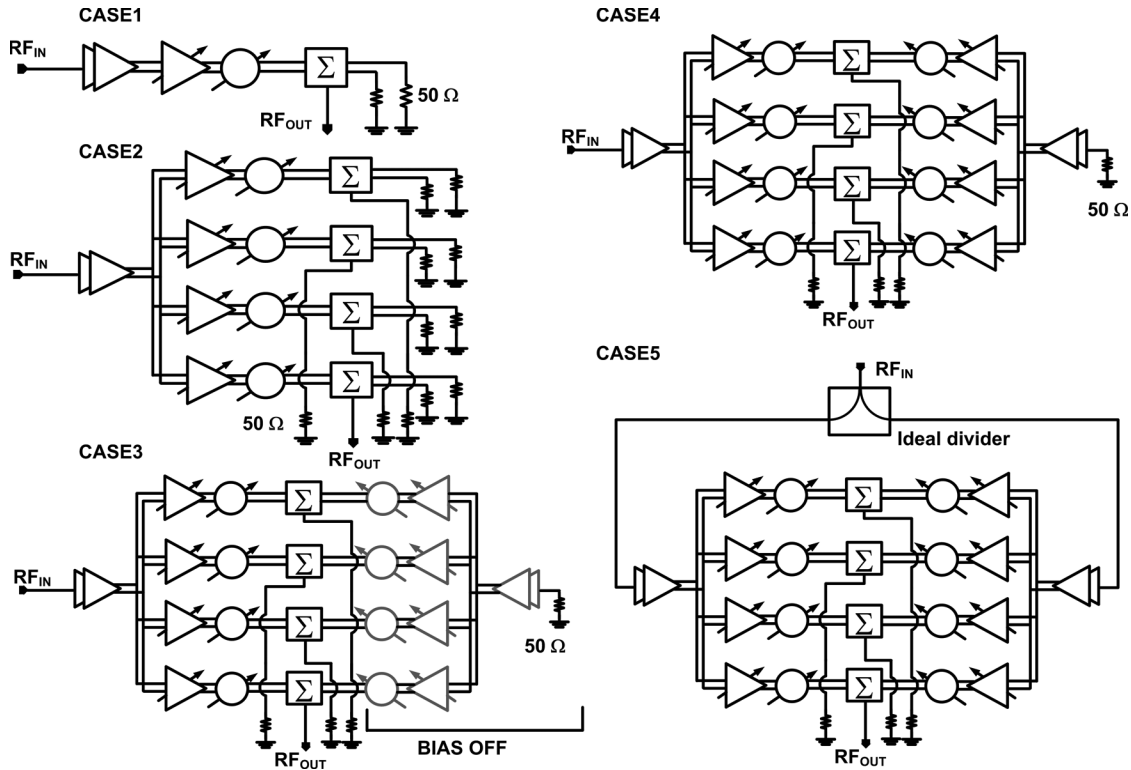


Fig. 5. NF case studies for the two-antenna and four-beam receiver.

Section II presents the details of the proposed phased array system, specific building block designs, implementation details, and noise figure (NF) investigation. Section III presents single-channel results and their comparison with simulations, presents variable gain amplifier (VGA) control, $P_{1\text{ dB}}$, third-order intercept point (IP3), and NF, and characterizes the beam to beam coupling at the S -parameter level.

II. SYSTEM LEVEL AND BUILDING BLOCK DESIGN

The operation of the chip is as follows [see Fig. 1(b)]: the input signal from each antenna is first fed to a low-noise active balun (LNAB) for differential signal processing. The LNAB is composed of a two-stage single-ended to differential converter. The signal is then split into four different paths using a differential splitter, and each path contains amplitude and phase control circuitry. The phase control is realized using vector modulation, commonly referred to as a phase interpolation technique [2]. The amplitude control is achieved using a 1-bit gain control in the signal splitting network and 3-bit gain control in the vector modulator (i.e., phase shifter). The signals from antenna 1 are then added to the corresponding signals from antenna 2 using on-chip differential active power combiners. The final “beam” outputs are single ended and this is achieved by internally terminating one port of the differential power combiners with $50\ \Omega$. This incurs a 3-dB penalty in the gain and output power, but eliminates active or passive baluns at the output ports, and therefore, ensures high isolation between the different output beams.

A. RF Building Blocks

The circuit level implementation is shown in Figs. 2 and 3. The LNAB is a two-stage emitter coupled amplifier with an

inductive load and de- Q resistors for wideband operation. The first stage provides low-noise amplification, input matching, and single-to differential signal conversion. The emitter length of $Q1$ is chosen as $20.3\ \mu\text{m}$ (emitter width = $0.2\ \mu\text{m}$) to minimize base resistance. The following stage results in additional common-mode rejection and low-noise amplification. The output differential emitter follower drives a passive 1:4 differential network with a differential impedance of $100\ \Omega$. This network is implemented using the top metal layers as a ground-signal-signal-ground (GSSG) topology and is simulated as a five-port network using full-wave techniques. There are four crossovers that are implemented using metal 5 and metal 6 (Fig. 2). The crossover area is $12 \times 10\ \mu\text{m}^2$ with a $2\text{-}\mu\text{m}$ oxide gap. This results in a crossover capacitance of $\sim 2.2\ \text{fF}$ and isolation over 40 dB at 13–15 GHz, and does not affect the differential operation.

A shunt inductor ($L = 0.14\ \text{nH}$) is placed at the output of LNAB to tune out the large parasitic capacitance of the 1:4 distribution network and the input stage of the following amplifier. The simulated differential load impedance at the output of the LNAB is $140\ \Omega$ at 14 GHz. The LNAB consumes 25 mA and results in a simulated gain and NF of 10.2 and 4.6 dB, respectively, at 13–15 GHz, when loaded with $140\ \Omega$ (i.e., not including the 1:4 distribution network loss). When it is loaded with the 1:4 distribution followed by the input impedance of the next stage, the simulated gain is 14 dB due to the increase in the load impedance. The simulated S_{11} is $< -10\ \text{dB}$ from 12 to 19 GHz.

The 1:4 distribution network is connected to differential cascode amplifiers to result in high isolation between the four channels. Gain control is achieved by steering the bias current of the common-base amplifier in the cascode stage using $Q1$ and $Q2$,

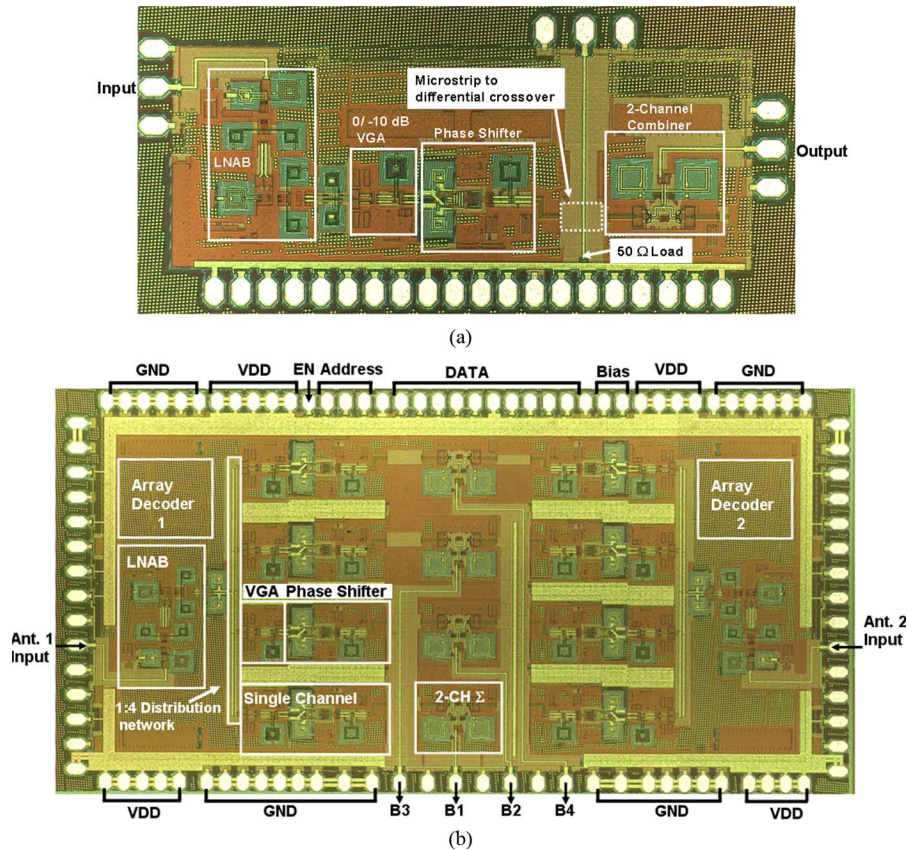


Fig. 6. Microphotographs of: (a) single-element ($2.4 \times 1.1 \text{ mm}^2$) and (b) two-antenna four beam ($2.4 \times 4.3 \text{ mm}^2$). The single element contains a microstrip to differential-line crossover so as to emulate the two-antenna four-beam chip.

and ensures minimal phase variation versus gain setting. The cascode amplifiers also show a high internal isolation so that one can implement a 1-bit gain control of $0/-10 \text{ dB}$ without affecting the input impedance (and thus, the 1:4 power division ratio). The cascode stage is followed by a differential emitter follower with 4.5 mA of bias current per path so as to drive the low-impedance (23Ω) all-pass in-phase/quadrature (I/Q) network. The simulated voltage gain is $-5/-15 \text{ dB}$ at $14\text{--}15 \text{ GHz}$ with a bias current of 17.4 mA . The NF referenced to the input of the VGA stage is 16 dB at 15 GHz when this stage is loaded with the input impedance of the following phase shifter. There is an option to shut off the entire RF path by turning off all the current sources in this stage ($Q3$ off). This is necessary in dual-polarized systems so as to be able to synthesize a vertically or horizontally polarized signal in a specific beam.

The overall gain and NF for LNA, 1:4 distribution network, and the $0/-10\text{-dB}$ VGA result in $9.1 \sim 8.8 \text{ dB}$, $6.4 \sim 6.3 \text{ dB}$, respectively, at $14\text{--}15 \text{ GHz}$ for channel 1 and 4. The gain is $\sim 1 \text{ dB}$ higher for channels 2 and 3 due to the additional length in the 1:4 distribution network. The simulated input $P_{1 \text{ dB}}$ is -19 dBm for channels 1 and 4 and -18 dBm for channels 2 and 3. The input $P_{1 \text{ dB}}$ is limited by the low load impedance, which is the input impedance of the quadrature all-pass filter (QAF).

The phase shifter is based on a $0.18\text{-}\mu\text{m}$ CMOS vector modulator with 4-bit DAC control. NMOS transistors are chosen for better linearity. The impedance of the QAF is

designed to be 23Ω with a resonance frequency at 15 GHz ($L = 180 \text{ pH}$, $C = 360 \text{ fF}$, $2R = 47.2 \Omega$). This results in $\leq 3^\circ$ of I/Q phase error under $\sim 100 \text{ fF}$ of loading capacitance, which corresponds to the gate-source capacitance of the vector modulator MOSFETs [2]. The size of these transistors ($W/L = 40/0.18$) is optimized for NF and linearity. A 3-bit amplitude control ($-1.25/-2.5/-5 \text{ dB}$) using current steering is achieved using PMOS loads and NMOS transistors operating in the linear region. The NMOS ($Q_{N0} \sim Q_{N2}$) transistors serve as digital switches and the PMOS (Q_{P1} , Q_{P2}) transistors are scaled $\times 2$ and $\times 4$ larger than the Q_{P0} for the 3-bit operation. Again, inductive loads are used with de-Q resistors for wideband operation. The simulated maximum gain and NF is $2.3\text{--}1.7$ and $9.7\text{--}10 \text{ dB}$, respectively, at $14\text{--}15 \text{ GHz}$. The phase shifter consumes 12 mA with a simulated rms phase and gain error of 5° , and 0.8 dB at 15 GHz , respectively. The gain error results from the amplitude mismatch (1.8 dB) resulting from the all-pass QAF and the quantization error of the 4-bit DAC. The simulated input IP3 of the vector modulator is $+12 \text{ dBm}$ at 15 GHz .

The vector modulator output is connected to a differential active combiner. The common source stage is again implemented using NMOS transistors for better linearity. As mentioned above, this combiner is designed to result in a single-ended output with a high isolation between the different combiners. This stage consumes 24 mA with a simulated gain of $\sim -1 \text{ dB}$ (one RF input with the other input terminated by 50Ω) and

~ 5 dB (two RF inputs) at 14–15 GHz. Notice that the (power) gain increases by 6 dB when two inputs are present since this is a current summer and is an active combiner. This is in contrast to a passive Wilkinson combiner with a power gain of 3 dB when two inputs are present. The simulated NF of the active combiner is 11 dB. The simulated output $P_{1\text{ dB}}$ with two inputs is -1.6 dBm at 15 GHz.

A $50\text{-}\Omega$ microstrip line connects the active combiner output to the edge of the silicon chip. As shown in Fig. 4, this topology results in several crossovers in the layout and it is imperative to minimize the coupling between the different RF paths. This is done by: 1) using a single-ended output over differential transmission lines and 2) using a localized M4 shield between the two sets of lines. The simulated isolation between the differential line ($Z_{\text{diff}} = 100\ \Omega$) and the $50\text{-}\Omega$ single-ended line is > 60 dB at 13–15 GHz. Referring to Fig. 1(b), in order to ensure symmetry in the difference paths, the output crossovers are implemented in all paths even if some paths do not intersect an output microstrip line. The overall system gain and NF is $9.7 \sim 9.2$ dB and $8\text{--}9$ dB, respectively, at 14–15 GHz for channels 1 and 4. The gain can be controlled by 18 dB using 4 bits with levels of $-1.25/ -2.5/ -5/ -10$ dB.

B. Overall Linearity

The simulated linearity of a single channel is limited by the QAF due to its low input impedance. The simulated input $P_{1\text{ dB}}$ is ~ -20 dBm at 15 GHz. When RF signals are present at both antenna ports, the input $P_{1\text{ dB}}$ is -20.2 dBm (for each port), resulting in an output $P_{1\text{ dB}}$ of ~ -6 dBm at each beam output. This indicates that the output active combiner does not enter into compression even with two input signals, and the linearity is still limited by the VGA/QAF stage.

C. NF Investigation

In order to characterize the NF of an RF channel in the four-beam chip, an S -parameter based SPECTRE noise simulation is done for the cases shown in Fig. 5. The simulated NF at 15 GHz of case 1 (8.06 dB) is almost same as that of case 2 (8.03 dB) and case 3 (8.15 dB). The slight difference is due to different impedances seen by the LNA and the output combiner. On the other hand, the NF of case 4 is ~ 11 dB and is due to the additional noise from the second antenna input, which is added at the combiner. Note that a hot/cold load is not presented at antenna port 2. This is an unrealistic NF and should not be used. Case 5 represents an actual phased array system where two RF inputs are used and are added coherently using the active combiner. In this case, the simulated NF is 7.77 dB at 15 GHz. This NF is 0.3 dB less than case 1 since the gain is higher by 3 dB (3-dB loss at the external power divider, 6-dB gain at the active combiner). Practical on-chip NF measurements can be done using case 1 (single element), case 3, and case 4, but it is seen that case 4 results in a nonaccurate characterization of the system NF.

D. Digital Control

The 4-bit phase and amplitude data for each path are loaded on the chip by an enabling clock signal and address decoders. The DAC and encoding logic are implemented using $0.35\text{-}\mu\text{m}$

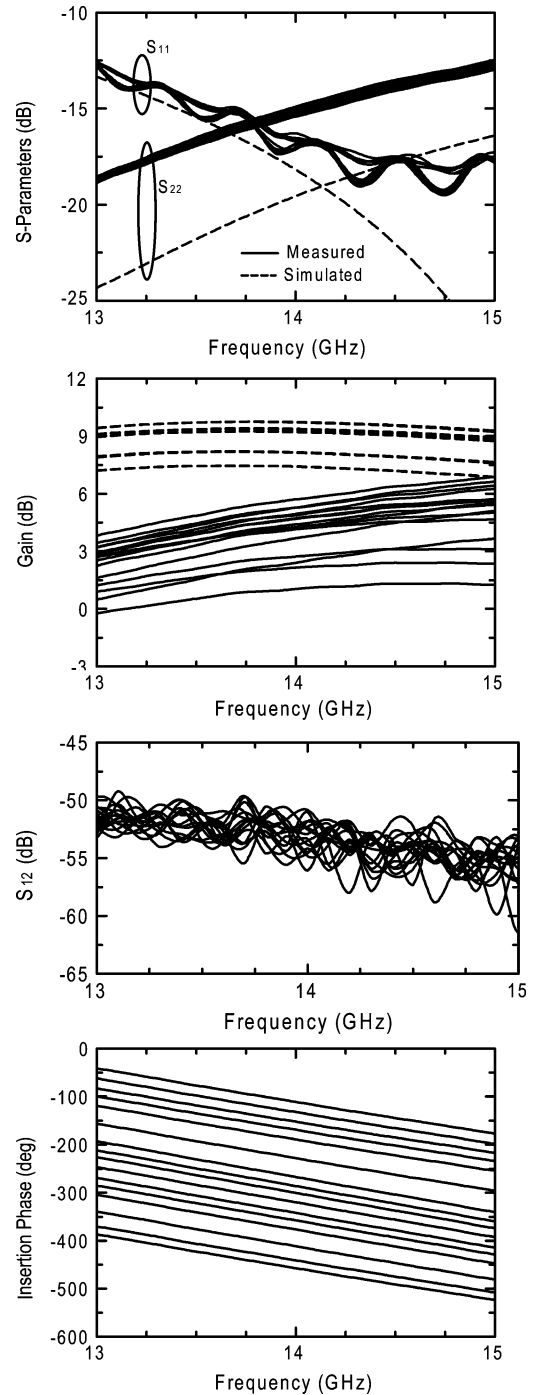


Fig. 7. Measured S -parameters of the single-element phased array for 16 phase states.

CMOS transistors. The phase and gain are set independently using a 9-bit digital data input (4-bit phase data, 4-bit VGA data, and 1-bit ON-OFF) to a shift register memory. A 3-bit data address is also required for the 3-to-8 decoder, which allocates an address to each register. The data is loaded by an enabling clock signal. The digital interconnection lines are realized with Metal 2 or Metal 3 for signal routing, and shielded by Metal 1 and Metal 4 ground planes to isolate the digital switching noise from the analog paths. Metal 1 is also used for the digital V_{DD} and it is separated from the analog V_{DD} (Metal 5) by the Metal 4 ground.

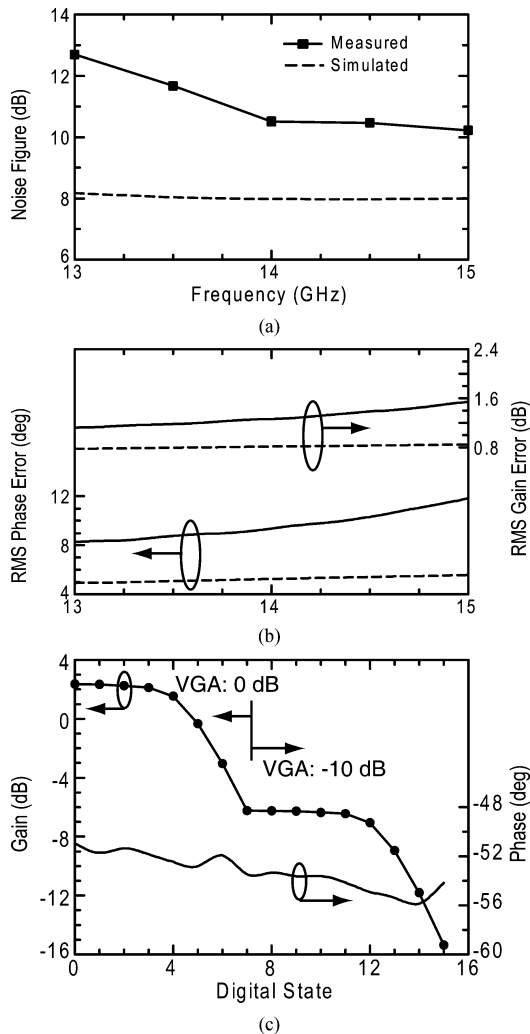


Fig. 8. Measured: (a) NF, (b) rms phase and gain errors, and (c) VGA gain control and associated change in phase shift at 14 GHz.

E. Chip Layout

The two-antenna four-beam phased array chip is implemented using the Jazz Semiconductor SBC18HX process with six metal layers. This process has $0.2\text{-}\mu\text{m}$ SiGe HBT (f_T of 155 GHz) and $0.18\text{-}\mu\text{m}$ CMOS transistors (f_T of 50–60 GHz). The RF channels are isolated from each other using a ground metal barrier, which is composed of a via stack from Metal 5 to Metal 1. In this region, V_{DD} is moved to Metal 6. For added isolation, a differential topology is used, the two antenna inputs are placed on the opposite sides of the chip, and the four single-ended $50\text{-}\Omega$ output lines are placed far away from each other. A ground metal barrier (Metal 6–Metal 4) is also used between the output microstrip lines of “beam 2” and “beam 4” in order to reduce the coupling [see Fig. 6(b)].

Jazz Semiconductor electrostatic discharge (ESD) protection diodes were placed at the RF input and output ports (1.6 kV, 1.1 A) and larger ESD diodes are placed on the digital control ports (3 kV, 2 A). Standard Jazz Semiconductor transistor cells and models are used, and full electromagnetic modeling is done on all the inductors and transmission-lines using Sonnet.¹ Over 100 pF of distributed de-coupling metal–insulator–metal (MIM)

¹Sonnet, version 11.52, Sonnet Software Inc., Syracuse, NY, 1986–2007

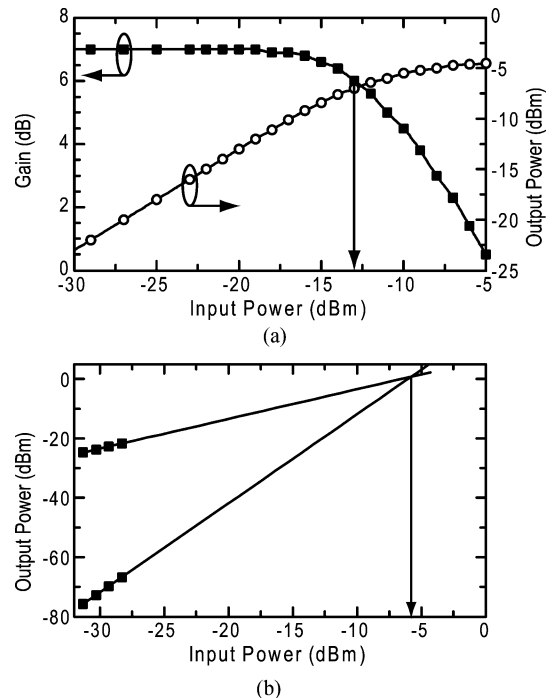


Fig. 9. Measured: (a) input $P_{1\text{ dB}}$ and (b) input IP3 of single channel at 15 GHz. The input $P_{1\text{ dB}}$ and IP3 are ~ 0.5 dB better at 14 GHz.

capacitors are placed on-chip between the VDD (Metal 5) and ground (Metal 4) to enhance the isolation between the channels. The chip dimensions are $2.4 \times 1.1\text{ mm}^2$ (single-channel prototype) and $2.4 \times 4.3\text{ mm}^2$ (two-antenna four-beam chip). The single-ended prototype contains a two-channel combiner with channel 2 input terminated in $100\text{-}\Omega$ differential. The simulated power consumption is 276 mW and 1.8 W, respectively, from a 3.5-V supply voltage.

All RF pads (two input and four output pads) are designed for $150\text{-}\mu\text{m}$ pitch ground–signal–ground (GSG) probes. All simulations include the pad capacitance and ESD effects.

III. MEASUREMENTS

The phased array chips were measured on-chip after a standard probe-tip short-open-load-thru (SOLT) calibration. The control inputs are supply voltage, address bits (3 bits), data bits (9 bits), and enabling clock signal to load the data to the registers. All measurements include the GSG pad capacitance and ESD effects.

A. Single-Channel Phased Array (Reference Design)

Fig. 7 presents the measured S -parameters of the single-beam chip over the 16 different phase states. The measured S_{11} and S_{22} are < -12.5 dB at 13–15 GHz. The measured gain is 4–6 dB lower than simulations depending on the frequency. The measured reverse isolation (S_{12}) is > 50 dB.

The measured NF is 10–11 dB at 13.75–15 GHz and is ~ 2 dB higher than simulated due to the lower channel gain [see Fig. 8(a)]. The measured rms phase error is $< 12^\circ$ up to 15 GHz showing 4-bit performance over an instantaneous bandwidth of 2 GHz, i.e., the phase error is less than half of the least significant bit [see Fig. 8(b)]. The measured VGA [see

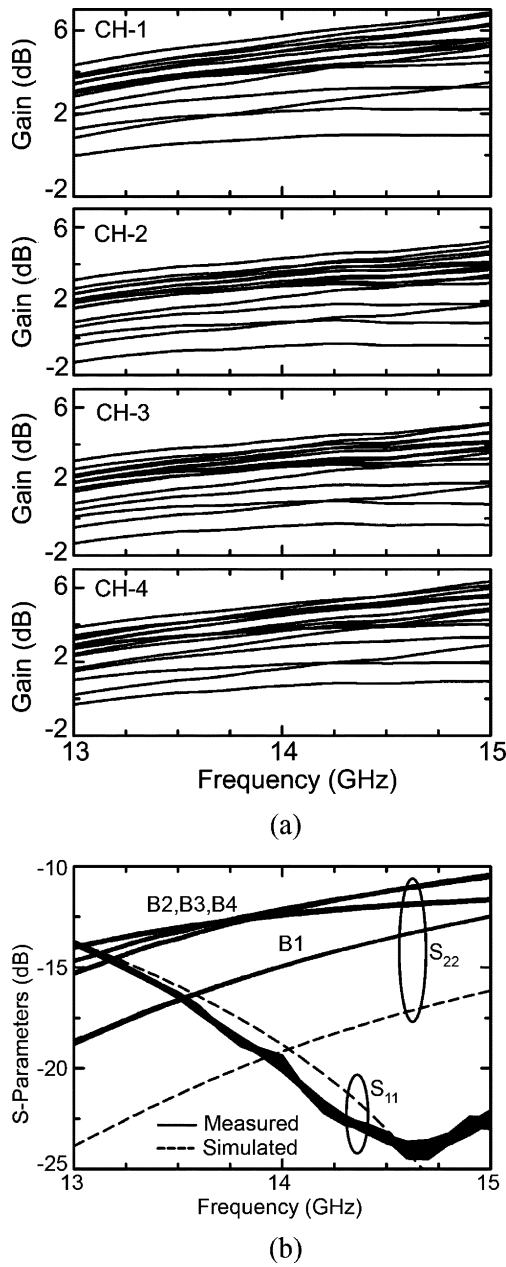


Fig. 10. Measured S -parameters of four-beam phased array for 16 phase states. (a) Gain. (b) S_{11} and S_{22} .

Fig. 8(c)] shows 17.6 dB of gain variation with 4-bit control, which is very close to simulations. The VGA insertion phase changes only by 5° with gain control. Hence, the VGA can not only be used for amplitude control (low sidelobe arrays), but also to compensate for the 1.5-dB rms gain variation in the phase shifter without changing the phase. The measured input $P_{1\text{ dB}}$ and input IP3 are -13.3 and -6 dBm, respectively, at 15 GHz at the maximum gain setting (Fig. 9). These are ~ 6 dB better than simulated due to the lower measured gain.

The discrepancy in gain, rms values, and NF is due to unexpected coupling between the 0.65-nH differential load inductor present at the output of the 0/ -10 -dB VGA and the QAF inductors. This coupling was not modeled, and in hindsight, it would have been better to either separate these inductors by an

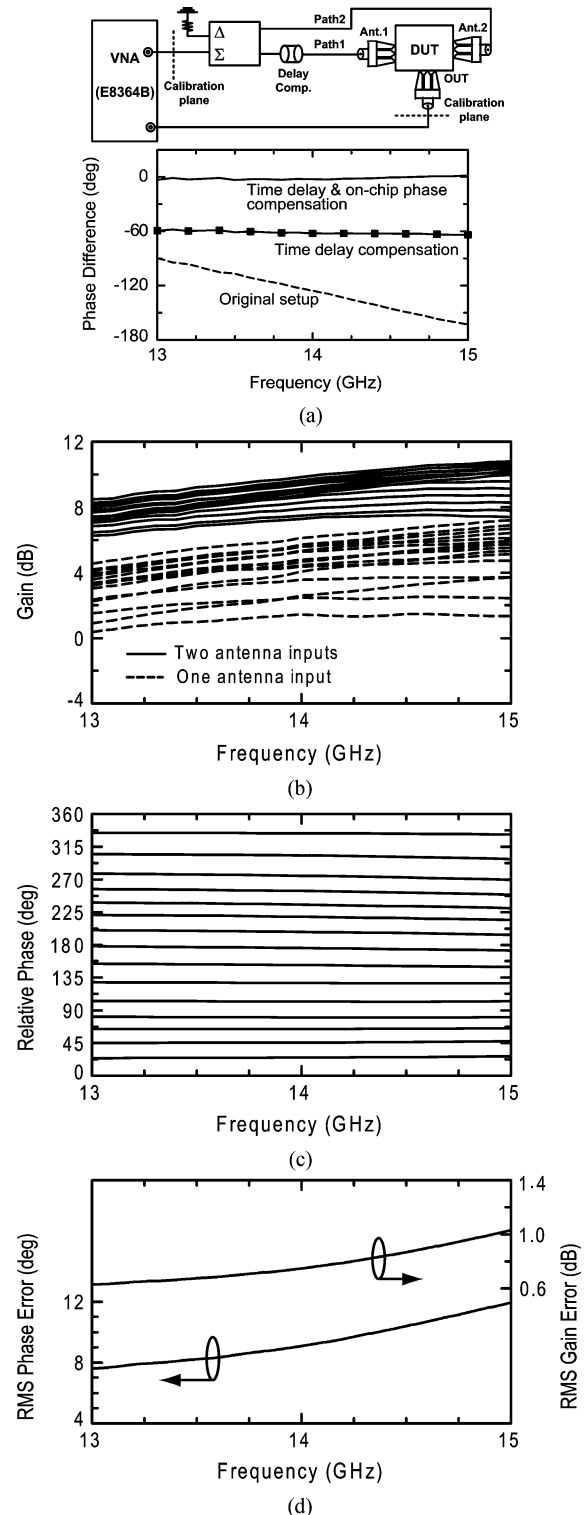


Fig. 11. (a) Experimental setup for input RF signals at both antenna ports. (b) Measured gain. (c) Relative phase response. (d) RMS phase and gain errors.

additional $100\ \mu\text{m}$ or to use two symmetrical inductors for the 0.65 nH in place of a single differential inductor.

B. Two-Antenna Four-Beam Phased Array

Fig. 10 presents the measured gain response for channels 1–4 for an input at antenna port 1 and with a $50\text{-}\Omega$ load at port 2. In these measurements, a single GSG probe was used for the

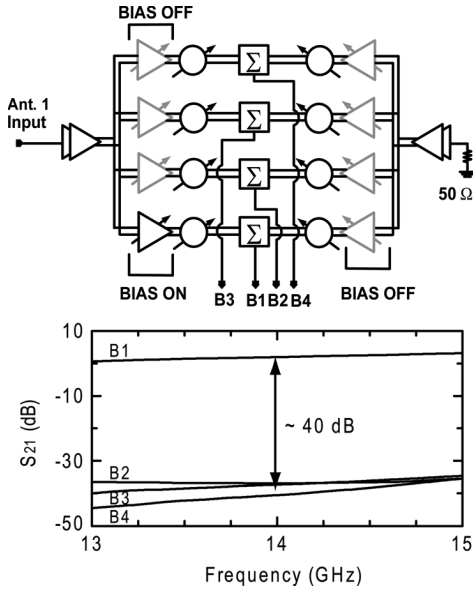


Fig. 12. Measured isolation for an input at antenna 1 and only channel 1 turned on.

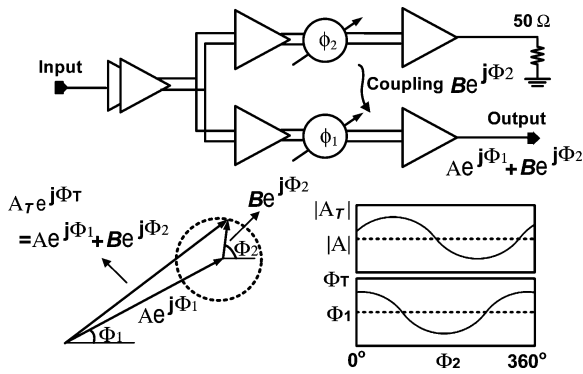


Fig. 13. Coupling characterization between two adjacent channels.

output port, and therefore, the nonmeasured channels were left open circuited, which presents a worst case condition in terms of coupling. The measurements result in very similar response between all beams over all phase states. The gain difference (0.5 ~ 1 dB) between channels 1 and 4 is due to the length difference in the 50-Ω output microstrip lines and the unequal loading effect by the 1:4 distribution network. The measured rms phase and gain errors for all channels are very similar to the single channel response and are not shown (within 1° and 0.1 dB). The measured S_{11} is the same as the single channel, but the output S_{22} for B1–B4 are slightly different due to the length difference among the output lines [see Fig. 10(b)]. The measured input $P_{1\text{ dB}}$ and input IP3 for a single channel is -12.3 ± 2 and -5 ± 2 dBm, respectively, at 15 GHz for different phase settings (worst case is input $P_{1\text{ dB}}$ of -14.3 dBm and IP3 of -7 dBm).

Virtually identical measurements were achieved for channels 1–4 for an input at antenna port 2 and with a 50-Ω load at antenna port 1. These measurements are not shown for brevity.

Fig. 11(a) shows the experiment setup to measure the S -parameters for input RF signals at both antenna ports. The gain is measured by de-embedding the coupler and cable losses. It is

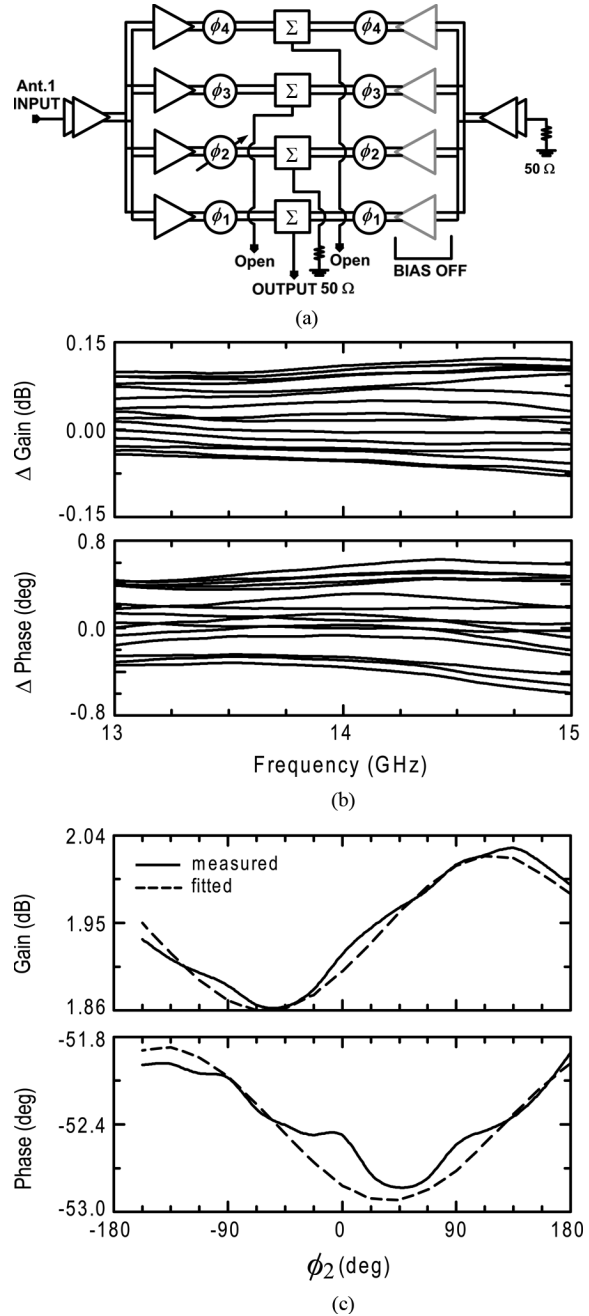


Fig. 14. (a) Coupling measurement setup with ant.1 input only. (b) Measured phase and gain errors versus -180° to $+180^\circ$ phase change in ϕ_2 ($\phi_1, \phi_3, \phi_4 = \text{constant}$). (c) Measured and fitted phase and gain errors versus the phase change at 14 GHz (fitted coupling vector magnitude, $B/A = 0.0092$).

important to equalize the phase and cable loss between path1 and path2, and two 3.5-mm adaptors are added to path1 so as to compensate the time-delay difference between the two paths (~ 100 ps). The finer phase adjustment is then done on-chip using the vector modulators. The measured gain increased by ~ 5 dB over a single channel. The 1-dB discrepancy (5 dB instead of 6 dB) is due to different phase settings in the single-antenna case and the two-antenna experiment, leading to a 1-dB drop in the channel gains. The measured rms phase and gain errors are $< 12^\circ$ and 1 dB, respectively, for the two-antenna

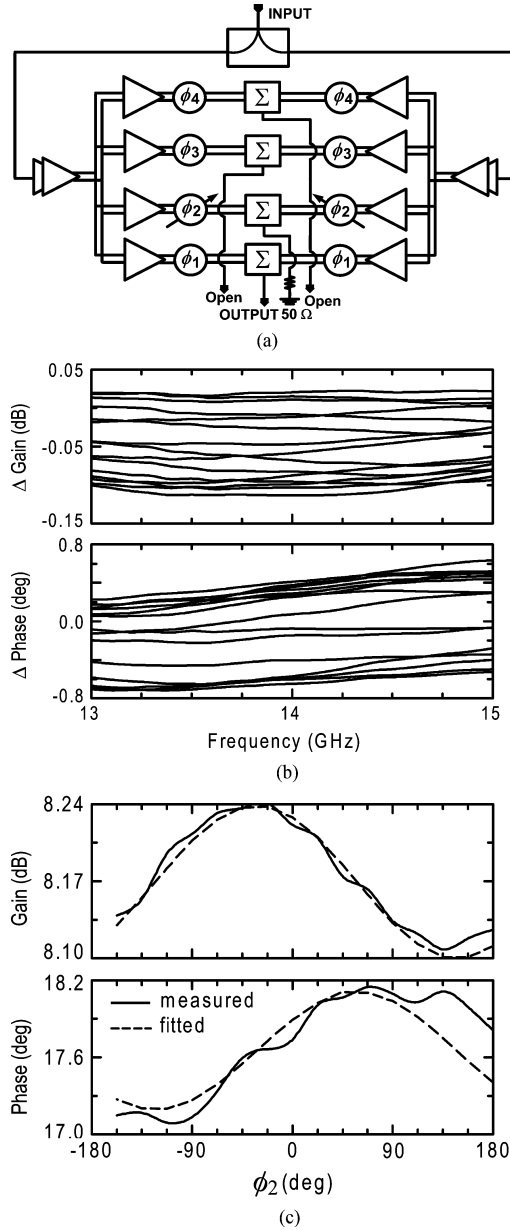


Fig. 15. (a) Coupling measurement setup with ant.1 and ant.2 inputs. (b) Measured phase and gain errors versus -180° to $+180^\circ$ phase change in ϕ_2 ($\phi_1, \phi_3, \phi_4 = \text{constant}$). (c) Measured and fitted phase and gain errors versus the phase change at 14 GHz (fitted coupling vector magnitude, $B/A = 0.008$).

experiment [see Fig. 11(d)]. The linearity also can be measured using this setup and the input $P_{1 \text{ dB}}$ is -14.6 ± 1 dBm at 15 GHz (at each port) over all phase states. The measured output $P_{1 \text{ dB}}$ is -5 dBm.

C. On-Chip Coupling Measurements

Fig. 12 presents the measured S_{21} for each channel for an antenna 1 input and the VGA in channel 1 turned on (all other VGAs are off). All other channels not connected to the measured port are left open circuited. The measured isolation is > 35 dB at 13–15 GHz (> 40 dB at 14–15 GHz). The same experiment was done on antenna 2 with similar results (not shown for brevity).

Accurate characterization of the coupling is also obtained by measuring channel 1 at a fixed phase setting and changing the phase in channel 2 from 0° to 337.5° , as shown in Fig. 13. Every channel from antenna input 1 (or antenna input 2) contains the same signal as the desired path due to the input signal divider, and any leakage from an adjacent channel to the desired channel can significantly affect the output amplitude and phase. As shown in the vector representation of Fig. 13, the output signal can be expressed as $A \exp(j\Phi_1) + B \exp(j\Phi_2)$, where A and Φ_1 are the desired gain and phase, and B and Φ_2 are the coupled gain and phase from the unwanted path. The maximum gain error is $A \pm B$ and occurs when $\Phi_2 = \Phi_1 \pm n\pi$ ($n = 0, 1, 2, \dots$). The voltage coupling vector magnitude $\alpha = B/A$ can be derived as

$$C = \frac{A - B}{A + B} \text{ and } \alpha = \frac{1 - C}{1 + C}. \quad (1)$$

The coupling phase (Φ_2) is the sum of a fixed phase offset (θ_0) and a phase shift (ϕ_2) of the phase shifter. Therefore, the measured gain and phase at the output can be fitted using

$$S_{21} = A \left[e^{j\Phi_1} + \alpha e^{j(\beta_0 + \phi_2)} \right]. \quad (2)$$

Fig. 14(a) shows the coupling measurement for an input at antenna 1 and the VGAs in antenna 2 are all off. The output of B2 is loaded by 50Ω , while the outputs of the B3 and B4 are left open circuited (a ground–signal–ground–signal–ground (GSGSG) probe used). The measured gain and phase deviation are $< \pm 0.1$ dB and $\pm 0.5^\circ$, respectively, at 13–15 GHz for a ϕ_2 change of 0° to 337.5° [see Fig. 14(b)]. Fig. 14(c) shows that the measured gain and phase errors as a function of a ϕ_2 change at 14 GHz, and are fitted using (2). The coupling vector magnitude is $\alpha = 0.0092$ (-40.7 dB). Similar experiments done with B1 output and varying channel 3 (ϕ_3) and channel 4 (ϕ_4) result in $\alpha = 0.0092$ (-40.7 dB) and $\alpha = 0.0029$ (-50.7 dB), respectively. These results are not shown for brevity. The results show that the channel-to-channel coupling is compatible with the straightforward measurements of Fig. 12.

Fig. 15(a) presents a similar experiment, but with two antenna inputs. The measured coupling factor for an output at B1 and varying ϕ_2 in both antenna paths is 0.008 (-42 dB) [see Fig. 15(c)]. The measured coupling factors for an output at B1 and varying ϕ_3 and ϕ_4 are 0.0046 (-46.7 dB) and 0.004 (-46.9 dB), respectively. Again, the coupling is very low.

IV. CONCLUSION

A Ku-band two-antenna phased array receiver chip capable of simultaneous four beams has been demonstrated in a $0.18\text{-}\mu\text{m}$ SiGe BiCMOS technology and successfully tested on-chip. The chip can be easily extended to eight simultaneous beams with little change in design or overall layout. Excellent beam-to-beam isolation was demonstrated using S -parameters and a system level test. The design can be scaled to Ka-band (35 GHz) or V-band (60 GHz) using a similar architecture for complex communication systems.

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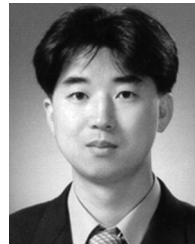
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