Performance and Modeling of Si and SiGe for Power Amplifiers

Pete Zampardi
peter.zampardi@skyworksinc.com

PA Pricing Roadmap

Price (¢)

Today's Price

In A Couple of Years, the PA WILL BE FREE

Time

Our GaAs Price Goes Down, Regular Gas Price Goes Up!

In a Few Years, We PAY for People To Use Our PAs!

What Is Important to a PA Customer?

- Meet All Specs – Over Temperature – Over Bias – Over Frequency
- Size (less space PAM takes up, more room for other stuff)
- The Customer
  - Requires Stable Supply of Parts
  - Wants Quick Response to Change in Volume Needs
  - Wants Low Power Consumption in PA Off Mode (Independent of RF input).
  - Wants No Extra Switches or Attenuators on the Phone Board
  - Wants Product to be Repeatable with Minimal Variation from Part to Part.
  - Demands Parts Stable in Operation with No Drift over Time.
- Some Customers Demand Viable Second Source for PA Manufacturing (Risk Reduction)
- End user really doesn't care about any of this!

Review of What is Going On

- Market moving away from stand-alone PAs
  - FEM's (consisting of multiple PA, switches, and controller's) are what customers are interested in
- Greater requirements for functionality
  - More intelligent bias circuits that are either controlled, or respond automatically to RF input signal and battery charge
  - Removal of isolators but PA required to (1) survive and (2) function over mismatch
- GaAs technology improvements
  - Die size reduction by improving packaging, pad sizes, and MIM cap densities
  - Addition of FET to allow more functionality in bias circuit
- Tangential features of the technology are why GaAs is ahead

PA Block Diagrams

Quad-Band GSM PA Module

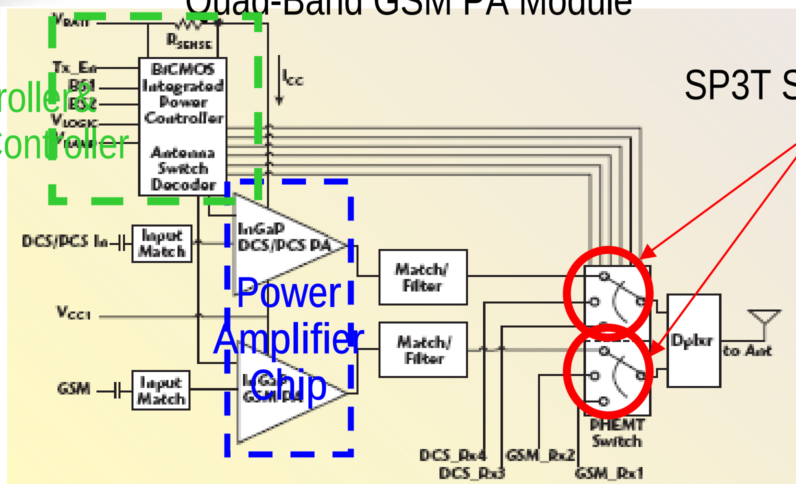
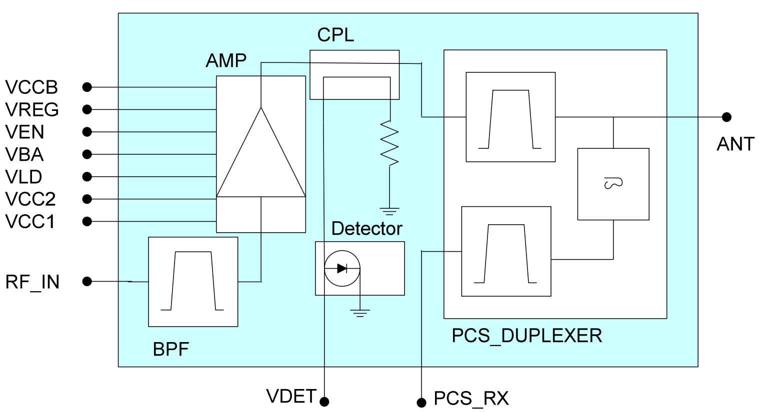


Fig. 1 Block diagram of the SKY77506 front-end module.

- GSM Module
  - Already some Si in there!
- Adding more bands/modes
  - Opportunities for Si due to partitioning



- PA Product Development is multidisciplinary, designer must be familiar with analog design, RF design, and be aware

- PA die is not only thing in there (percentage cost)
- Trade-offs abound

Specs & Requirements

- Frequency – must operate across a band, not single point
- Collector Voltage – a range (2.9 to 6)
- Bias Supply Voltage – a range (also low current draw)
- Output Power Minimum (-50) to Maximum (27, 29, 34 dBm)
- Power Gain (26 to 28 dBm)
- Gain Variation over Temp (-1 dBm to 1 dBm)
- ACP (1^{st} and 2^{nd}) and ACP under mismatch
- DC/DC Compatibility
- MSL Level
- ESD Robust
- Max Current
- Receive Band Noise
- Harmonics
- Leakage Currents
- Switching Time
- Stability, Control Slope
- Pad configuration

Research Papers Typically Only Report Stuff in RED and they usually quote ACP to the SYSTEM spec, not PA SPEC

- Many specifications besides Gain, PAE, and Linearity
- Not everything looks as good on Si as it does on paper

Si/SiGe/GaAs Results

Nellis, JSSC, 2003

TABLE VIII

MEASURED LOAD-PULL RESULTS OF Si AND GaAs PAs FOR POUT=28 dBm[1,2]

Technology	PAE (%)	ACPR1 (dBc)	ACPR2 (dBc)	P_{GAIN} (dB)
Si	44.2	-46	-54.9	30.5
	42.9	-47	-55.0	30.4
	41.5	-48	-55.0	30.4
	40.1	-49	-55.0	30.3
	38.5	-50	-55.0	30.2
GaAs	46.2	-46	-55.9	29.5
	44.8	-47	-56.1	29.4
	43.4	-48	-56.5	29.2
	42.1	-49	-56.9	29.1
	40.8	-50	-57.4	29.0

[1] V_{CC} = 3.4V, f_0 = 836.5MHz, IS-95 Modulation, Temp = 25°C
[2] For each ACPR1, the highest possible PAE was selected. For each ACPR1 and its highest PAE, the best tradeoff between P_{GAIN} and ACPR2 was made.

- **PA Level Load-pull**
- **GaAs PA outperforms Si, but Si is close.**

Si(Ge) Parts Were Rugged Enough to Pass Spec

Cell-band Good, PCS Bad

TABLE IV

MEASURED LOAD-PULL RESULTS OF Si, SiGe, AND GaAs PAs FOR POUT=28 dBm[1,2]

Technology	PAE (%)	ACPR1 (dBc)	ACPR2 (dBc)	P_{GAIN} (dB)
Si	33.9	-44	-57.0	22.0
	33.6	-45	-56.9	22.2
	33.1	-46	-56.8	22.3
	32.5	-47	-56.8	22.4
	31.6	-48	-56.8	22.5
SiGe	35.0	-44	-57.4	21.8
	34.2	-45	-57.2	22.2
	33.5	-46	-57.3	22.7
	32.5	-47	-57.5	22.4
	30.2	-48	-57.5	22.5
GaAs	43.6	-44	-59.2	26.6
	42.8	-45	-59.1	26.8
	41.9	-46	-59.2	26.9
	41.0	-47	-59.7	27.0
	40.0	-48	-60.1	27.1

[1] V_{CC} = 3.4V, f_0 = 1.88GHz, IS-95 Modulation, Temp = 25°C
[2] For each ACPR1, the highest possible PAE was selected. For each ACPR1 and its highest PAE, the best tradeoff between P_{GAIN} and ACPR2 was made.

- **PA Level Load-pull**
- **GaAs PA outperforms Si and SiGe PAs.**
- **Si and SiGe PAs perform comparably.**
- **SiGe <u>does not</u> offer any advantage over Si for PA applications.**

Si(Ge) vs. GaAs Status

- Si(Ge) is rugged enough for linear application
- Si(Ge) performance is adequate for linear 900 MHz operation
- Si(Ge) performance at 900 MHz for GSM not quite as good as GaAs
- Si(Ge) higher frequency performance insufficient for 1.9 GHz linear or saturated applications (for linear the gain is too low, for saturated the PAE is not nearly as good)
- Si(Ge) seems to be fine for some other "PA" applications and is doing okay there (WLAN, etc)

Si(Ge) Currently Does Not Have Much Market Traction for Handset PAs

Why ?

- Time To Customer
  - Turn-around time on GaAs HBT is ridiculously fast, so conversation starts sooner. Cost differential is also not as large as people think (it's not all about wafer costs, the die are really small). Specs ALWAYS change
- Supplier/Customer Relationship
  - Proven providers of handset PAs have provided good low cost, high volume solutions. Customer relationship is a big barrier to entry for fab-less guys (can they deliver?).
- Market Size
  - PA market is small (relative to markets Si is used to playing in) companies with dedicated Si(Ge) processes have not made the investment to make the "perfect" PA technology because they are making money other places.

Outline

- Introduction
- Changes Create Opportunities
  - LiPA
  - Mid-power Efficiency
  - Multi-mode/Multi-band
  - Lower Operating Voltage
- Technology Development Opportunities
  - Wafer Thinning & TWV
  - Precision passive components (R's & C's)
  - Interconnect Improvements
  - Transistor Level Improvements
- Modeling Challenges for PAs
  - Multiplicity Scaling
  - Interconnect
  - Thermal Design/Interactions
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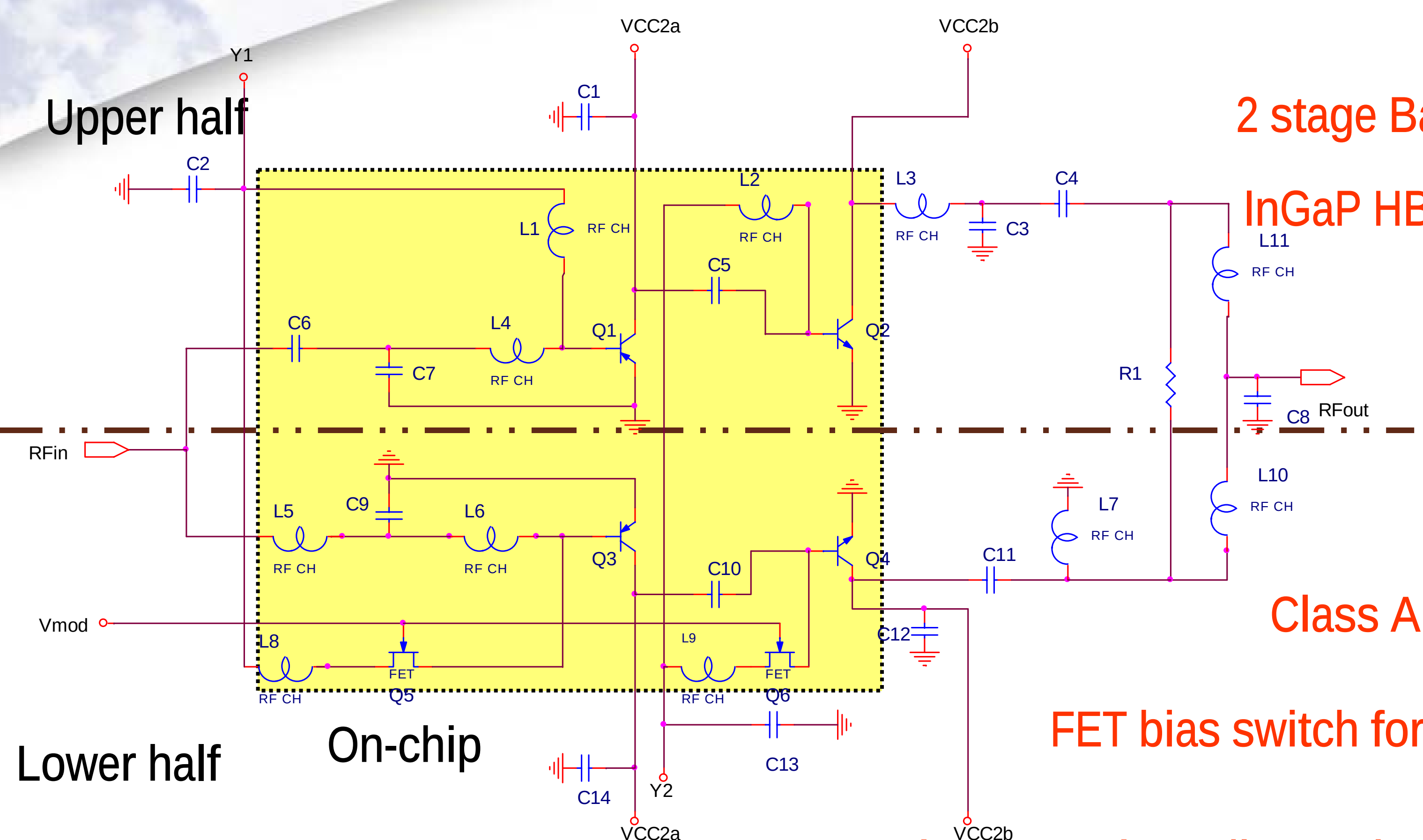
Load Insensitive PA

- Interesting contrast between Si approach and GaAs approach
- Goal is to allow removal of isolator
  - Part must still survive
  - Part must actually perform well over some specified mismatch region

Design of a Switched Load Insensitive Power Amplifier (LIPA®)



2 stage Balanced PA

InGaP HBT Technology

Class AB Operation

FET bias switch for mode control

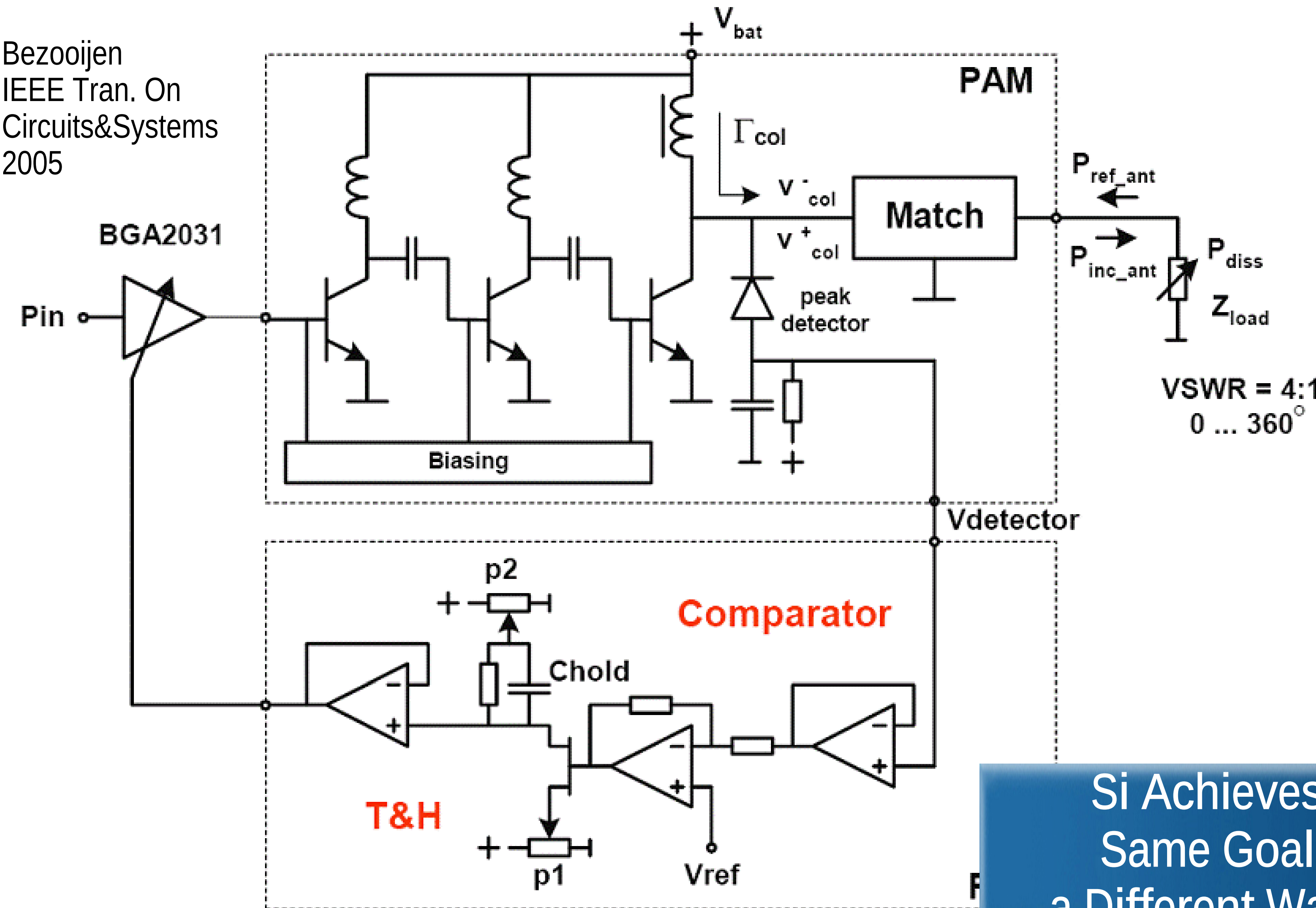
Analog control to adjust quiescent current

Zhang, 2006 RFIC

Lower half switched off @ low power mode

Adaptive PA used for measurements

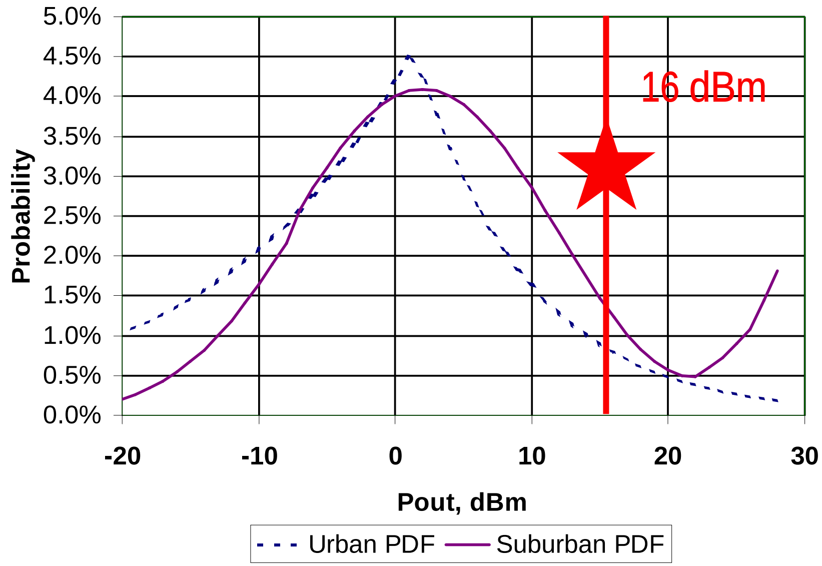
Bezooijen
IEEE Tran. On
Circuits&Systems
2005



Si Achieves Same Goal a Different Way!

Mid-Power Efficiency

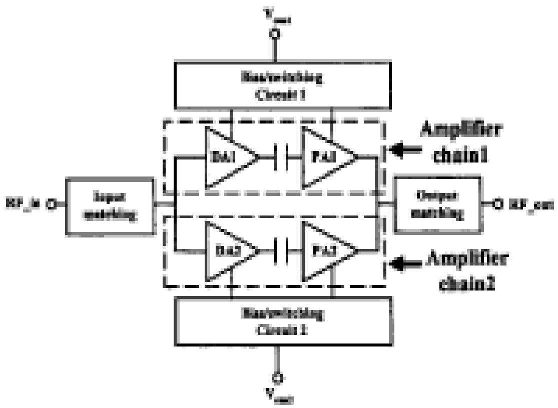
- Phone manufacturers are now benchmarking phones for linear applications at 16 dBm or "mid-power"
  - GaAs HBT/BiFET uses by-pass switch or parallel stage design
- This may create opportunities for Si(Ge) PAs
  - DC/DC integration with device (although not all manf. will use this) is possible.
  - CMOS switches may be sufficient for this application
  - Other "novel design" twists



- CDMA Development Group
  - Urban & Suburban Output Power Statistics
- Application to Power Amplifier
  - 5dB offset for worst case PCS losses between PA and antenna
  - 90% Operation 10dB to 17dB Below Rated Power
  - Low Power Efficiency Enhancement Statistically Significant

Mid-power Efficiency – Current Approaches

Kim, GaAs IC 2002



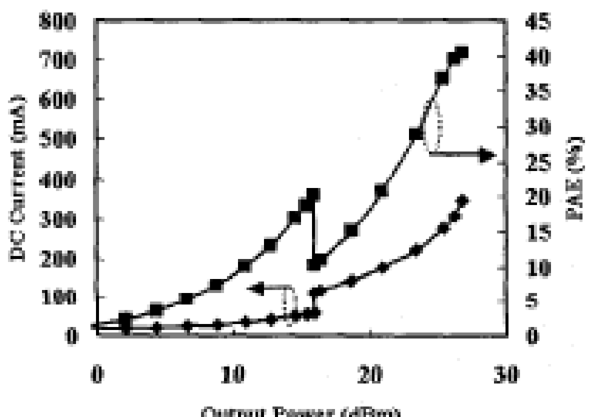
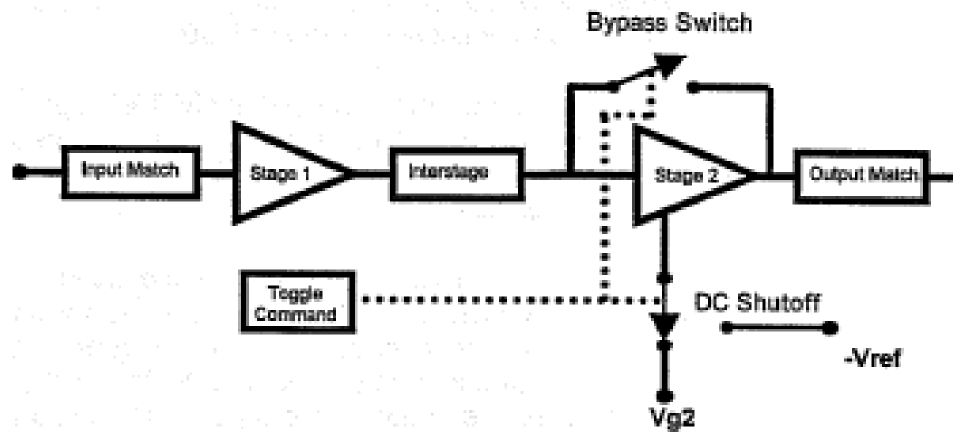
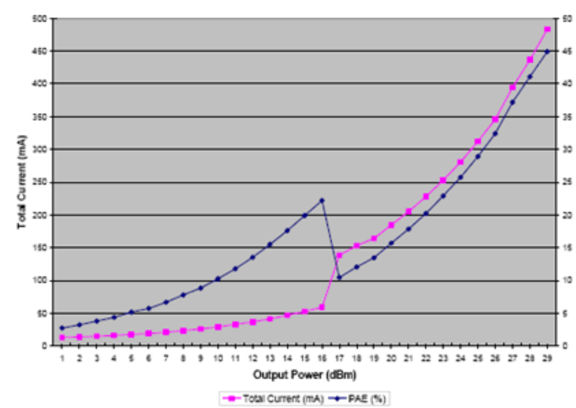


Figure 8. Measured DC current and power added efficiency of the dual chain MMIC power amplifier.

H. Patterson 2000 IEEE Topical Workshop on Power Amplifiers for Wireless Applications, paper 2.7





Example of HELP PA

BiCMOS and Mid-Power Efficiency

Huang and O, JSSC, March 2001

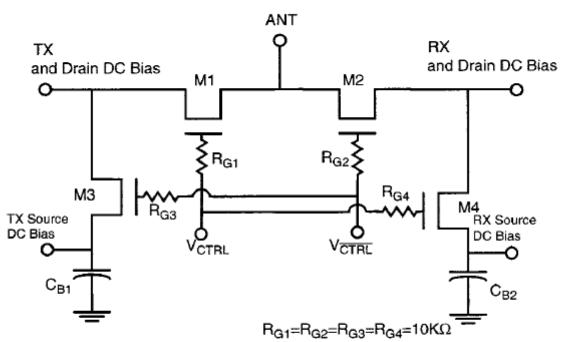


Fig. 1. Circuit schematic of an SPDT RF T/R switch.

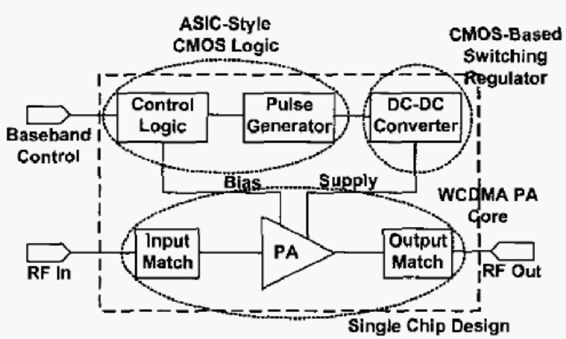


Fig. 1. System block diagram of a variable supply voltage power amplifier

Rippke, RFIC 2005

Deng, et al, MTT, Feb 2005

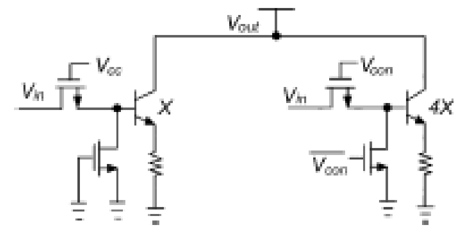


Fig. 11. Output stage transistors with DCB. HBTs are biased "on" or "off" in response to output power requirements.

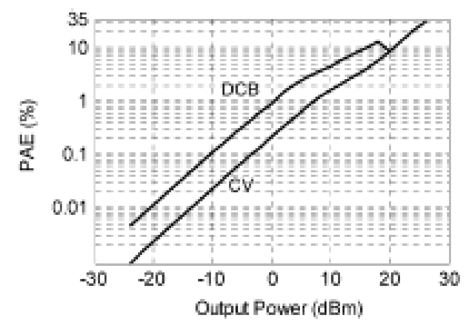


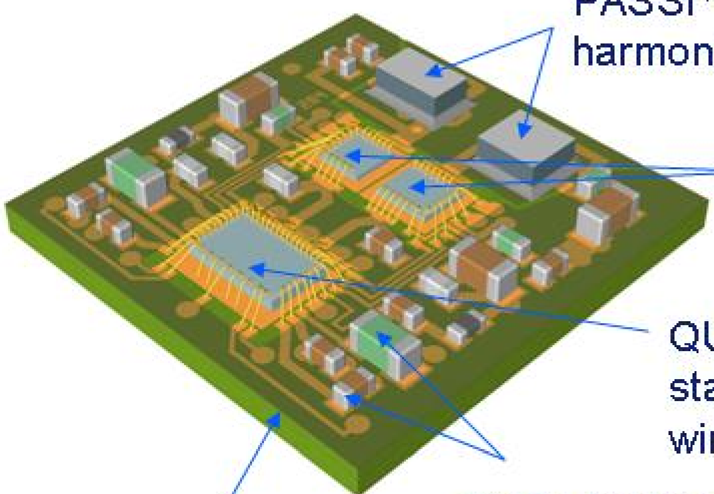
Fig. 18. Measured PAEs with *CV* with fixed area (*CV*) and DCB with varied area (DCB) PAs.

- CMOS Adequate for By-passing
- DC-DC Converter Integration Possible
- Other “switching” methods

Multi-technology SiP assembly platform

Application example in (quadband GSM) PA module BGY284

Molded package (not shown)



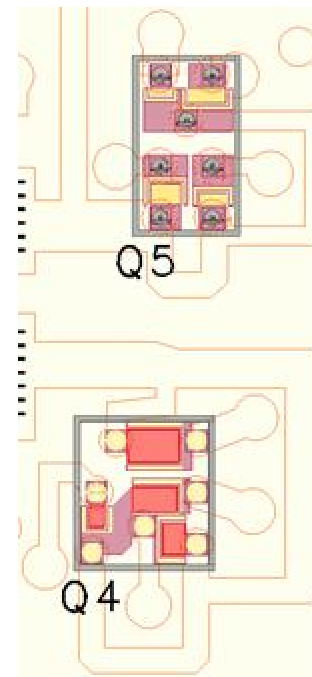
PASSI™ dies for output matching and harmonics filtering, flipchip-mounted

GaAs HBT dies for PA output stages, wirebonded

QUBiC die for PA first and intermediate stages, for biasing and for control, wirebonded

SMDs for low-frequency supply decoupling and for interstage matching circuits, soldered

Laminate substrate as mechanical carrier, I/O rerouting and collector feedlines



Layout of the two PASSI™ dies and their environment

Partitioning Includes More Si

Lower Operating Voltage

- Several Potential Issues and Questions
  - Questions
    - Does it still have to work on a 5 V charger (are we just making the range bigger?)?
    - Does it still have to deliver same maximum power?
  - Issues & Opportunties
    - Bias circuit design – easy for Si, not so easy for GaAs
    - PAE and Pout as a function of Vce (for fixed load-line)
    - Integrated Regulator in Si?

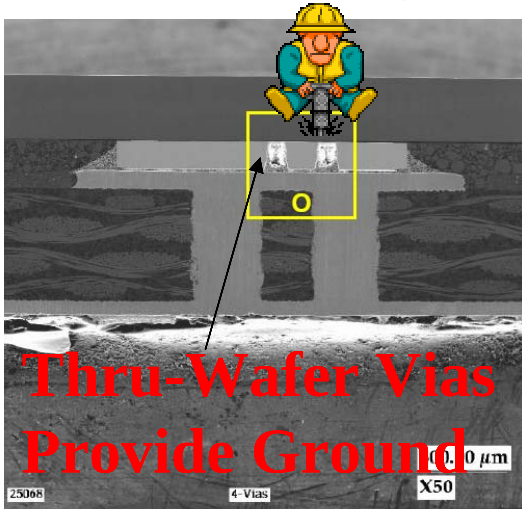
A Lower Battery Voltage Could Present a NICE Opportunity for Si

Outline

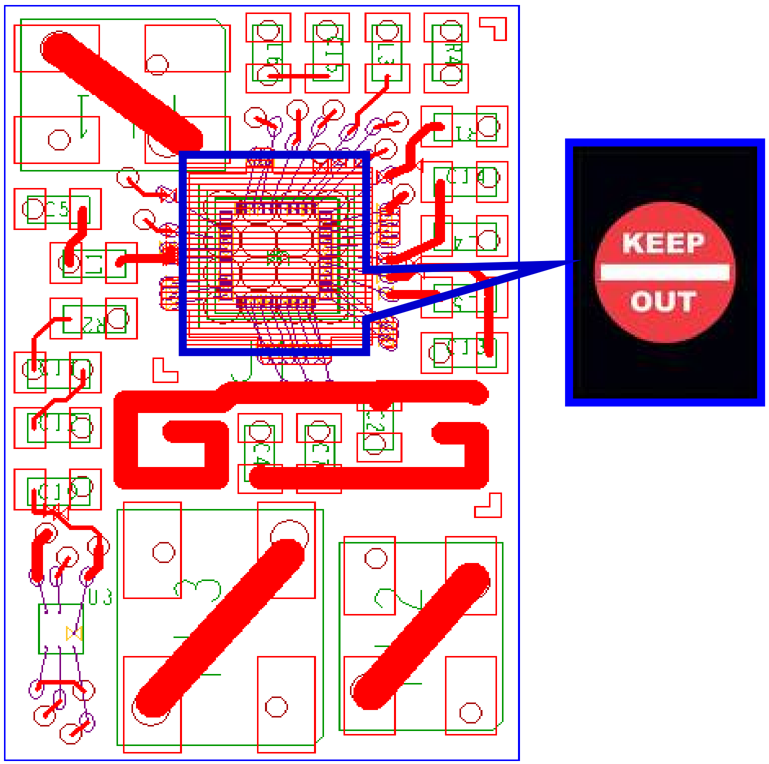
- Introduction
- Changes Create Opportunities
  - LiPA
  - Mid-power Efficiency
  - Multi-mode/Multi-band
  - Lower Operating Voltage
- Technology Development Opportunities
  - Wafer Thinning & TWV
  - Precision passive components (R's & C's)
  - Interconnect Improvements
  - Transistor Level Improvements
- Modeling Challenges for PAs
  - Multiplicity Scaling
  - Interconnect
  - Thermal Design/Interactions
- Summary

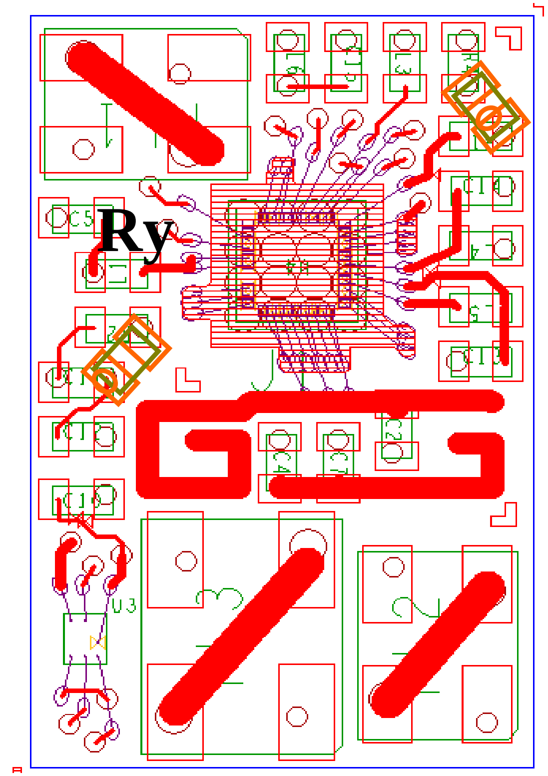
Through-Wafer-Via (TWV)

- TWVs provide:
  - Better Grounding (10-20 pH/Via, 4.5 mOhm) (higher gain), also more consistent
  - Smaller Die (eliminates ground pads)
  - Smaller Keep-out area around die = smaller module&shorter bond wires
  - Wafers thinned (4 mils) for this – shorter wires, thinner substrate
- Ground current does not need to route all the way out. Potentially smaller arrays (wiring is a limitation in arrays). Also lowers on-chip inductance
- No Si fab offers TWV (Philips/Delft have experimented with, others are too)
  - Wafer thinning typically only to 7-8 mils
  - Flip-chip with thermal management or aggressive die thinning is required
- Details that matter
  - Via size (resistance & inductance & size)
  - Via to via spacing
  - Via to pad and/or chip-edge
  - Via to device
  - Via shape



Practical Impact of Not Thinning





Thicker Die = Larger Keep Out Region
In this case, module (5x8) would not be DRC compliant!

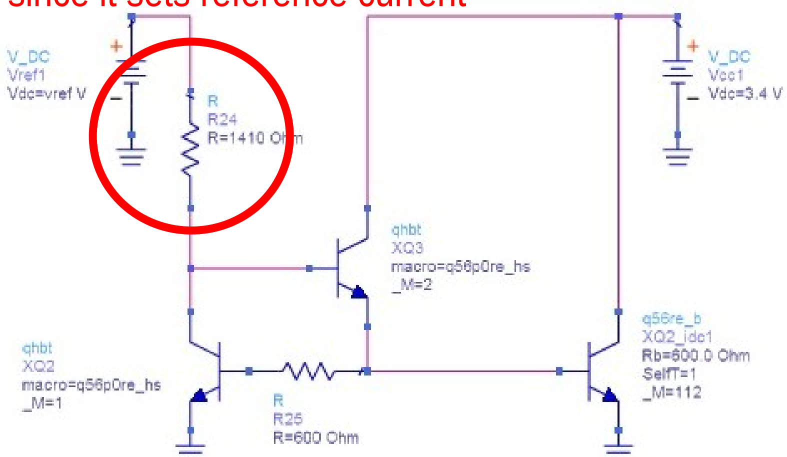
Die thinned to 4 mils, DRC compliant module!

Module Size Matters
Must Minimize PRODUCT Cost

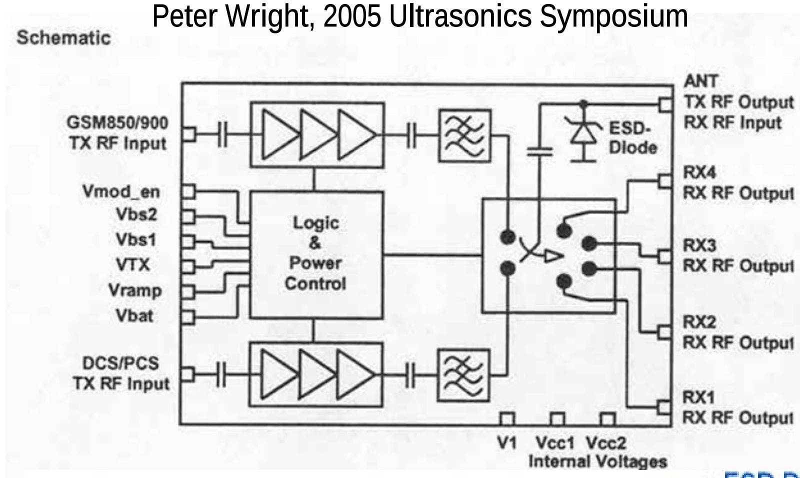
High Precision Passives

- For on-chip biased circuits, precision resistors are required to reduce product variation (<10%), also has a TCR~100 ppm
- MIM Capacitors are used for inter-stage matching (and sometimes for part of output match), also need high precision (<10%)

This resistor needs to be precise since it sets reference current



Peter Wright, 2005 Ultrasonics Symposium



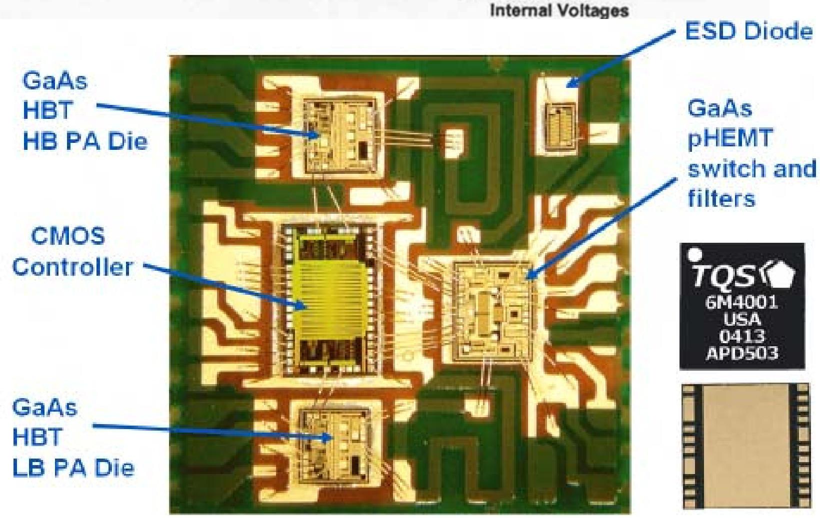
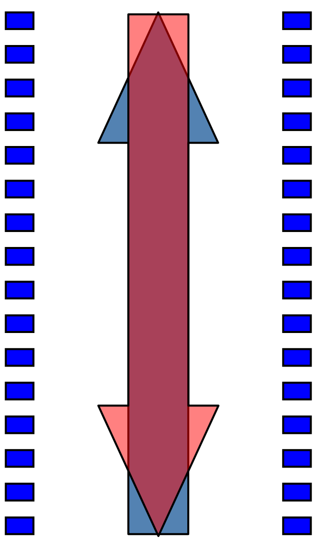


Figure 8. GSM quad-band transmit module

Precision Passives are Important!

Interconnects

- Current carrying ability has impact on array size (trade overlap cap and resistance)
- Inter-level dielectric THICKNESS is ALSO important (minimize capacitance)
- Au (on GaAs) very nice for thermally shunting transistors together



Bus width example

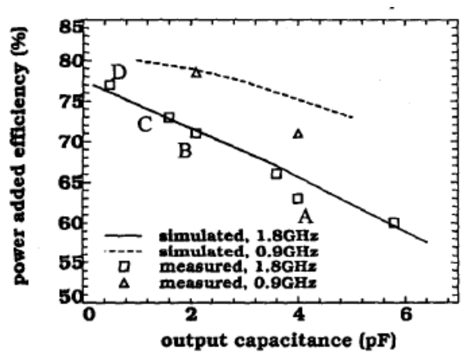


Figure 1: Power added efficiency as function of output capacitance.

Van Rijs 2000 MTT-S

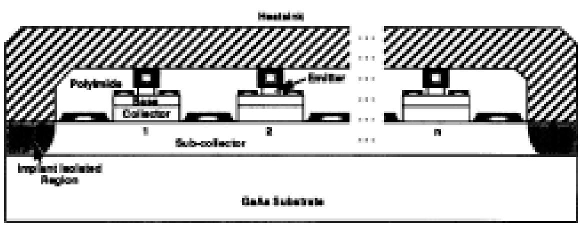
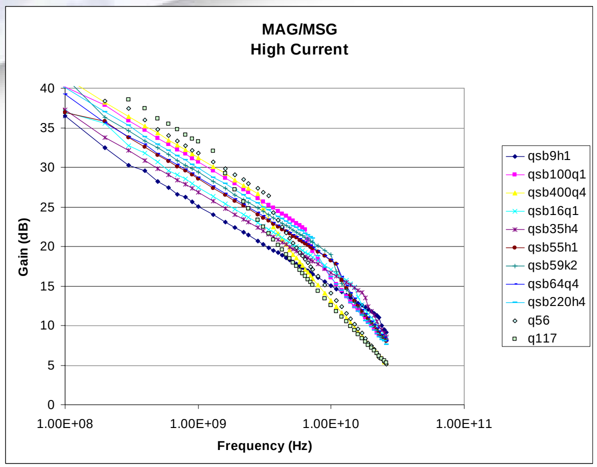


Figure 2b. xx' cross-sectional view of n base fingers of the device.

B. Bayraktaroglu *et al*, *1996 IEEE MTTS* pp.685-688.

Thermal Shunting Example

Transistor Offering Improvements



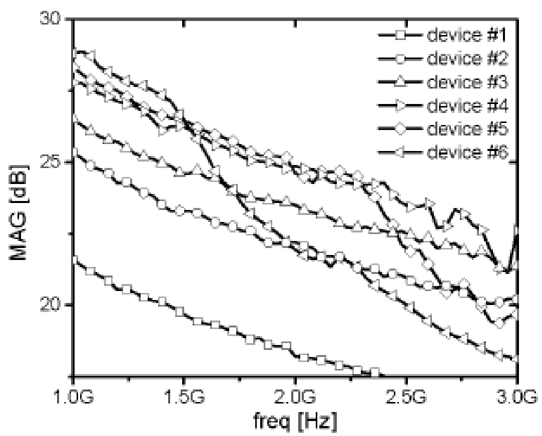
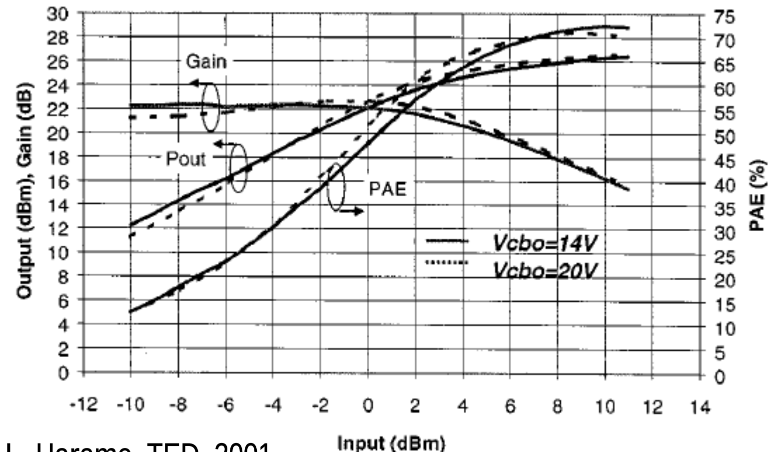


Fig. 4: Maximum stable gain (MSG) for the various device configurations.

Spirito
ISPSD 2006



D. L. Harame, TED, 2001

Fig. 23. Comparison of 900 MHz PA performance for 640 μm^2 power device in V_{cbo} = 14 V and V_{cbo} = 20 V technologies. The higher breakdown technology has nearly equivalent performance to the V_{cbo} = 14 V technology.

Rule of Thumb: BV_{ceo}~8, BV_{cbo}>20 V (GSM)
But: BVceo~5.5, BVcbo~14 (CDMA)
REALLY WANT BOTH OF THESE ON CHIP!

Narrowest Device, Not Always Best!
Wider Gives Smaller Array – Trade-off

Still Some Opportunity for Device/Technology Optimization

Deep Trench

- Addition of deep trench increases device thermal resistance
- Deep trench really not necessary for PA design, but if it is there, some flexibility is probably required.

Technology	R_{TH} (K/W)
No trench	860
Trench isolated	1420

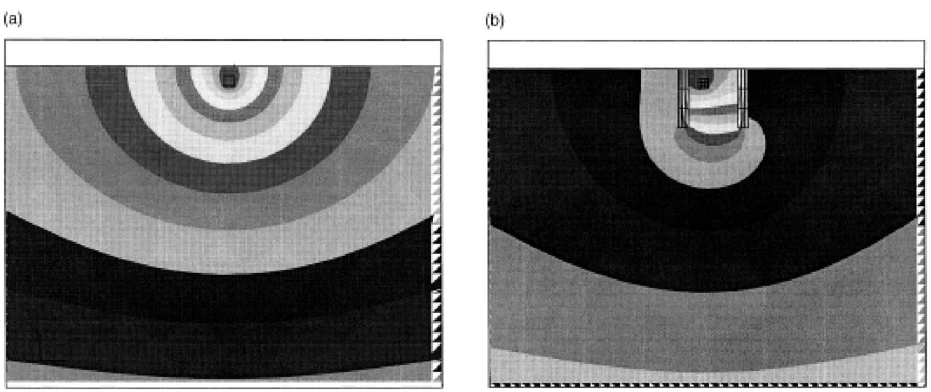
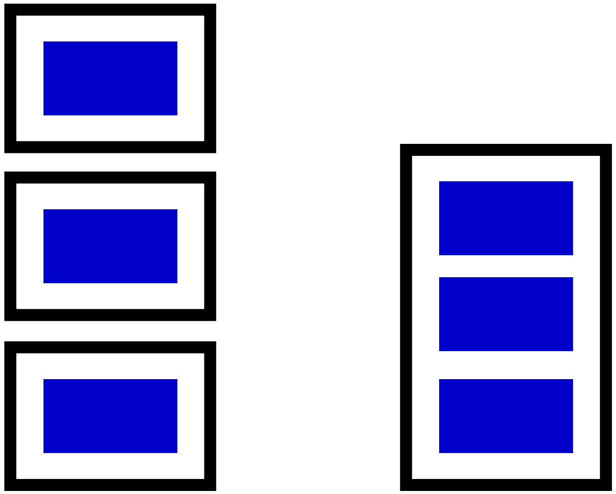


Fig. 2. Isotherms from numerical simulation (a) no trench present (max contour 75 and 5 K increments) (b) with trench (max contour 119 and 8 K increments).

Walkey, Solid State Electronics, 2000

Individual DT's Lead to Large Arrays



Deep Trench Can Be Optimized for Arrays/PA Applications

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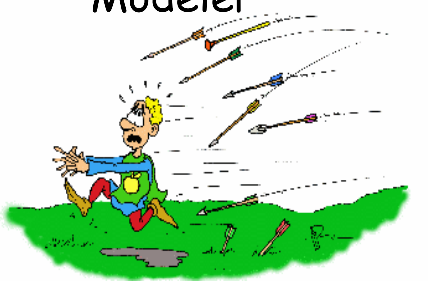
Modeling

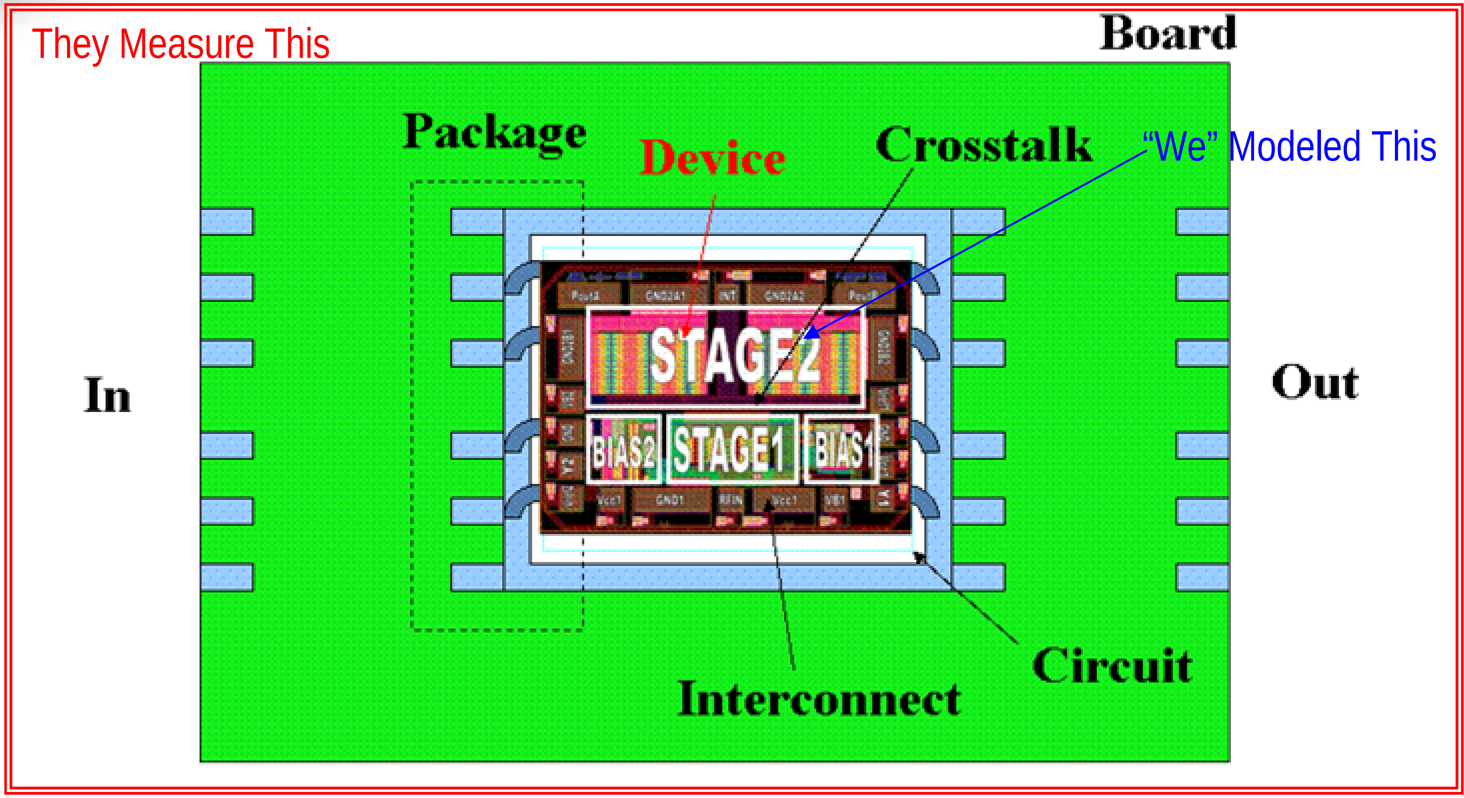
- Si(Ge) Compact Models are EXCELLENT! (VBIC, HiCUM, MEXTRAM, even SGP are all okay for designing PAs)
- However, PAs are a different animal than most circuits – high power, very non-linear operating regions, not stationary bias
- Device modeling generally stops at unit cell
  - PA designers consider the array a “device”, so array scaling is needed
    - Two main effects: (1) Electrical (interconnect) and (2) Thermal (device-device)
  - Since this is an “analog” circuit, thermal GRADIENTs are also important
  - Other stuff (like package, bondwire, etc) is also VERY important, but not discussed here

Key Consideration: Needs to integrate into design flow!

Designer View of Modeling

So…
Blame The
Device
Modeler

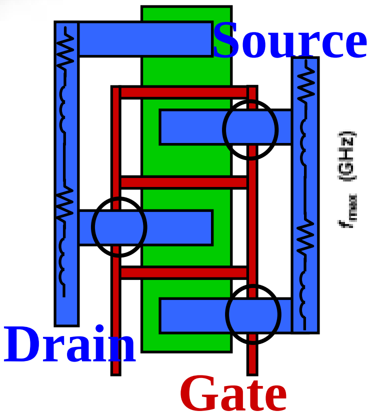


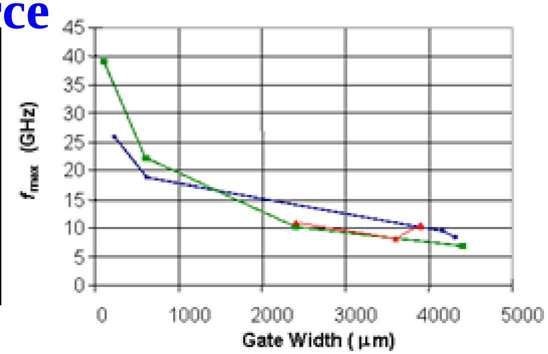


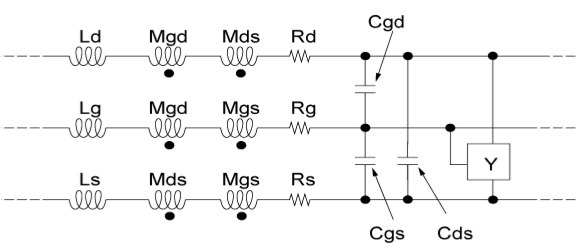
Device Modeling: Unit cell models that don’t depend on environment (no feedback from layout or simulator)
Circuit Modeling: Requires layout or simulation information

Crosstalk: Electrical & Thermal
Interconnect: RLC, not just RC

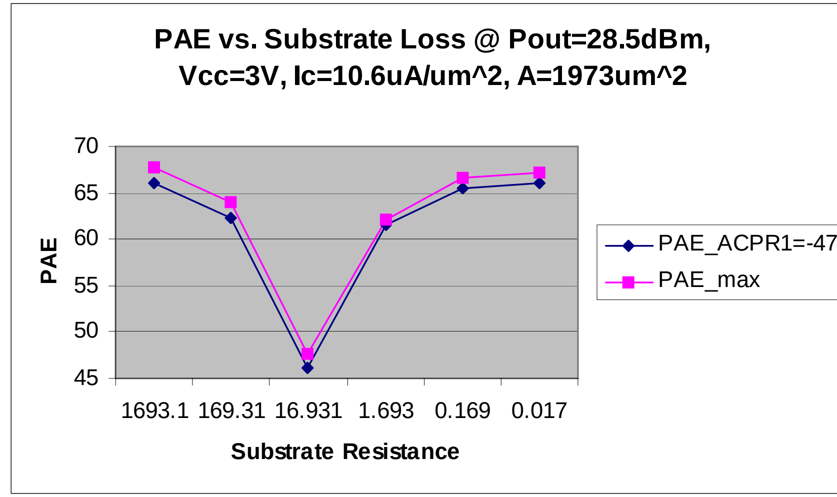
Interconnect Modeling







Wetzel, 2000 PA Workshop



On Si, poor routing choices over lossy-substrate need to be accounted for

Almost impossible to model every possible array, so EM simulation works well

- Lumped elements, t-line, or full EM all about same (from EM sims)

Interconnects MAY be important for particular designs

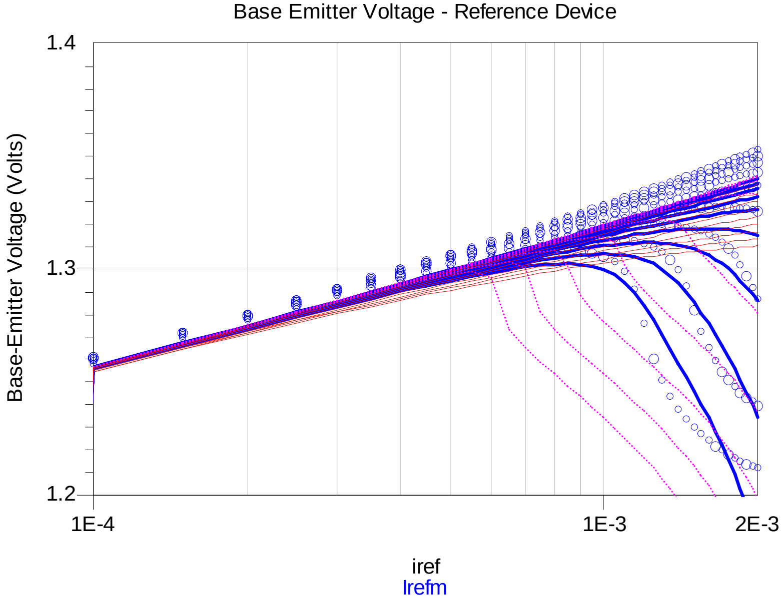
Temperature Modeling of Arrays

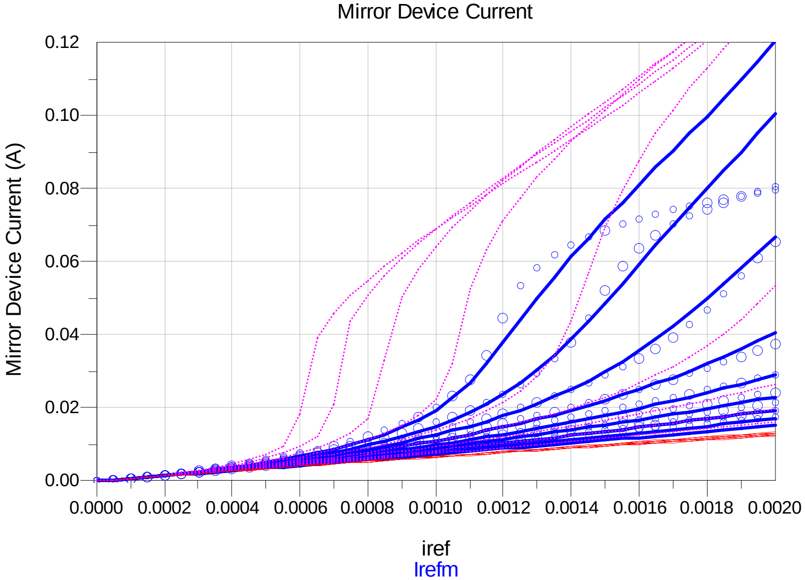
- Two reasons to consider
  - (1) SOA and
  - (2) electrical performance matching.

  - For SOA, looking of maximum temperature, for performance, a weighted average is needed.
- Issues:
  - R_{th} is typically a function of temperature (even for Si)
  - Temperature distribution changes across array with power
  - Dissipated Power is a function of both DC and RF power ($P_{dis}=P_{dc}+P_{in}-P_{out}$)
  - Generic "designer friendly" solution is needed
  - Depends on things external to the die (like epoxy/phone board)

Impact of Thermal Gradients

Q12 (reference) to Q117 (mirror)





Red Line = Perfect Coupling, Simulated
Blue Circles = Measured data
Blue Line = Simulated – Best Match, Simulated
Cyan Dash = No Coupling, Simulated

26 µm Separation, Measured vs. Simulated

- No thermal coupling gives significant error
- Perfect coupling okay for low V_{ce}'s

Some Nice Work on Thermal Modeling

A SPICE MODEL FOR PREDICTING STATIC THERMAL COUPLING BETWEEN BIPOLAR TRANSISTORS

Hélène Beckrich[(1)(2)], Thierry Schwartzmann[(1)], Didier Céli[(1)], Thomas Zimmer[(2)]

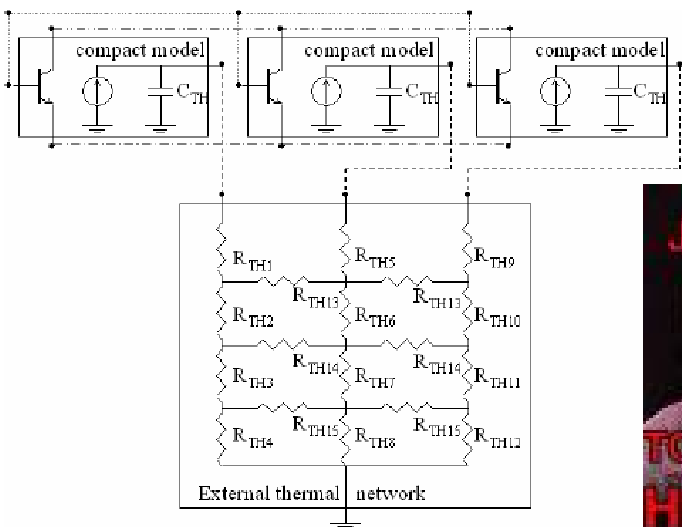


Figure 7. Thermal network implementation in a SPICE simulator. The transistors are connected by electrical and thermal nodes.

De Paola, ISPSD 2006

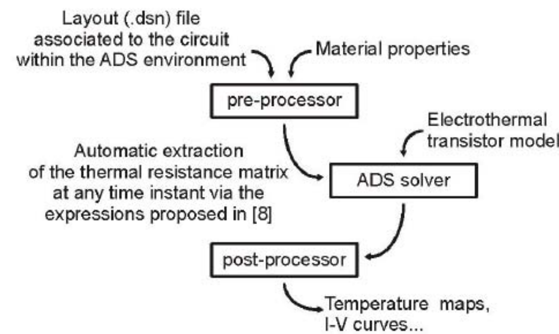


Fig. 1. Diagram flow of the ADS-based software.

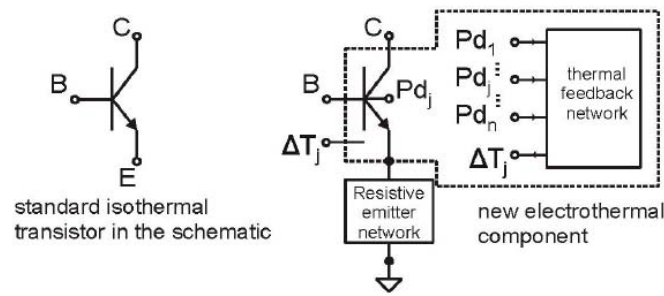


Fig. 2. Schematic representation of the purely isothermal device and the corresponding SDD (Symbolically Defined Device) component accounting for the electrothermal feedback.

Can be Auto-generated in TRADICA

Integrating Thermal in Design Flow is Key Challenge!

Summary

- The trend for higher levels of integration (multi-mode) may lead to higher levels of Si content in handset PAs
  - Multi-mode
  - Mid-power efficiency
  - DC/DC integration
  - User friendly features
- Some aspects of Si(Ge) technology improvement/refinement are still required for handsets (the CMOS has some requirements too)
- Compact device models are adequate, need to be extended to “circuit” level models for PA design simplification.

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Acknowledgments

- Keith Nellis
- Dr. Ken Weller
- Entire SWKS NBP Device Design, Characterization, and Modeling Team
- SWKS NBP Design Teams

Thank You!